INSTRUCTION MANUAL

MULTIPLEXER/
DEMULTIPLEXER
MA 1142
MA 1233

SANGAMO WESTON
Schlumberger

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EDITION AUGUST 77

OPERATING MANUAL

MULTIPLEXER/
DEMULTIPLEXER
MA 1142
MA 1233

SANGAMO DATA RECORDERS . P.O. BOX 3041 . SARASOTA, FLORIDA, 33578, USA
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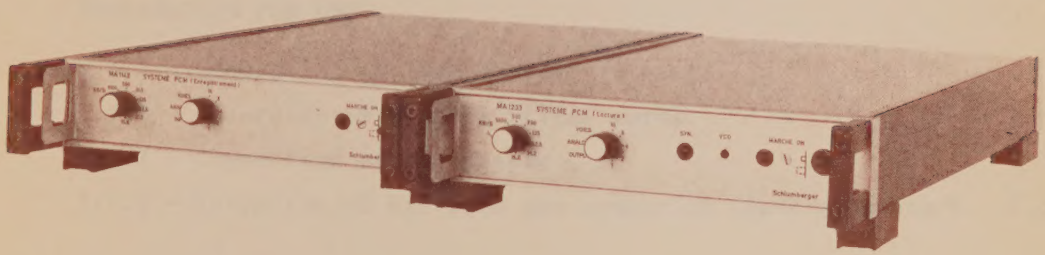
MA1233 SYSTEME PCM (Lecteur)
SYN
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MA 1142/MA 1233 MULTIPLEXER/DEMULTIPLEXER UNIT

MAGNETIC TAPE RECORDER ADAPTATION

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MA 1142/MA 1233 MULTIPLEXER/DEMULTIPLEXER UNIT

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CHAPTER I

GENERAL

1. PURPOSE

This analog input/output multiplexer system comprises two independent modules, the MA 1142 record module, and MA 1233 read module, combined mechanically to form a 19" standard module, height 1 U.

The equipment is designed for operation with any analog magnetic recorder, with channels equipped for the Direct mode.

This unit provides for simultaneous acquisition and restoration of 1, 2, 4, 8 or 16 parameters, with bandwidth up to 32 kHz for 1 parameter and 2 kHz for 16 parameters, where magnetic recorder bandwidth is 300 kHz.

The equipment provides a high degree of operational flexibility, particularly with respect to choice of bit rate and the number of parameters handled.

A number of options are available (input and output level, phase equalizer, record filters, terminal strip of multi-pin socket connection, etc.).

- Associated equipment
  - . Input card
  - . Input filter card
  - . Storage card
  - . Output filter card

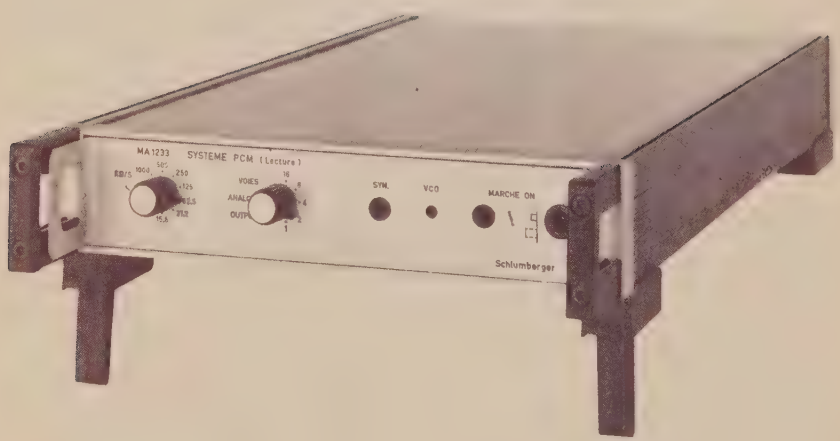


Fig.1 - Module pieds escamotables sortis

MODULE WITH FOLD AWAY FEET EXTENDED

1.2 - CHARACTERISTICS

1.2.1 - General characteristics

- Dimensions: 215 x 44.4 x 360 mm
  (two modules can be fitted side by side in a 19" standard rack, height 1 U).
  Height with fold-away feet extended: 97 mm.

- Power supply: 220/240 V (or 110/127 V, switched internally), 50 - 60 - 400 Hz.

- Consumption (with all filters):

  . MA 1142: max. 24 VA

  . MA 1233: max. 27 VA.

- Temperature:

  . Operation: 0° to +50°C

  . Storage: -55° to +125°C.

- Weight:

  . MA 1142: 3 kg

  . MA 1233: 3 kg.

1.2.2 - Measurement characteristics

1.2.2.1 - Record module

- Bit rate:
  Front panel selector: 1 M bit/s, 500 - 250 - 125 - 62.5 - 31.25 - 15.6 - 7.8 kbit/s.

- Number of parameters handled:
  Front panel selector: 16 - 8 - 4 - 2 - 1.

- Bandwidth:

Min. Recorder bandwidth (-3 dB)	Rate (kbit/s)	Bandwidth per channel				
		16 Channels	8 Channels	4 Channels	2 Channels	1 Channel
500 kHz	1000	2 kHz	4 kHz	8 kHz	16 kHz	32 kHz
250 kHz	500	1 kHz	2 kHz	4 kHz	8 kHz	16 kHz
125 kHz	250	500 Hz	1 kHz	2 kHz	4 kHz	8 kHz
62 kHz	125	250 Hz	500 Hz	1 kHz	2 kHz	4 kHz
31.2 kHz	62.5	125 Hz	250 Hz	500 Hz	1 kHz	2 kHz
15.6 kHz	31.2	60 Hz	125 Hz	250 Hz	500 Hz	1 kHz
7.8 kHz	15.6	30 Hz	60 Hz	125 Hz	250 Hz	500 Hz
3.9 kHz	7.8	15 Hz	30 Hz	60 Hz	125 Hz	250 Hz

- Bandwidth: { with read filter: +0.5/-1 dB
  with record and read filters: +1.5/-1 dB

- Input impedance for each channel:

  Zin: > 1 MΩ

- Nominal input voltage:

  ± 1 V (options: ± 2.5 V, ± 5 V, 0/+2 V, 0/+5 V).

- Max. input voltage:

  ± 5 V

- Record code:

  NRZL (spectral correction)

- Conversion: 10 data bits + 1 parity bit.

- Output impedance:

  Zout: approx. 50 Ω

- Nominal output level:

  2.8 V pp (option: adjustable up to 10 V pp).

- Filters:

  Plug-in cards, defined according to selected bit rate and number of channels (see table on page 1.3).

1.2.2.2 - Read module

- Input impedance:

  Zin: 10 kΩ paralleled by 100 pF.

- Nominal input level:

  2.8 V pp ± 3 dB (option: adjustable from 0.5 to 10 V pp)

- Phase equalizer incorporated (option), for utilization of the read module with a recorder the response curve of which is not phase-corrected.

- Bit rate
- Number of channels
- Output level

  } Same specifications as for record module

- Nominal output level:

  ± 1 V, 10 mA max. without filter (option: ± 2.5 V, ± 5 V, 0/+2 V, 0/+5 V).

- Filtered analog outputs:

  Plug-in filters, identical to those used for record, are defined according to bit rate and number of channels (see table on page 1.3).

- Stored analog outputs:

  These modules are defined according to bandwidth and for each channel:

  4 to 32 kHz
  1 to 2 kHz
  250 to 500 Hz
  15 to 125 Hz

- Relative differential phase-offset between two channels (with read filters)

$$F = Fc\ \emptyset \leq \pm 10^\circ \quad (Fc = \text{filter cut-off frequency})$$

$$F = \frac{Fc}{2}\ \emptyset \leq \pm 2^\circ$$

- S/N ratio (thermal noise):

$\geq$ 60 dB (with Vout = 5 V in 0 - 1 MHz band)

- Digital output on 25-pin connector:

. 10 data bits
. 4 address bits + 1 enabling bit } TTL level

- Resolution:

$\pm$ 1/2 increment (0.001% of measurement range)

- Thermal stability for record/read:

70 ppm/°C of measurement range (without filter).

CHAPTER II

PREPARATION FOR USE

UTILIZATION

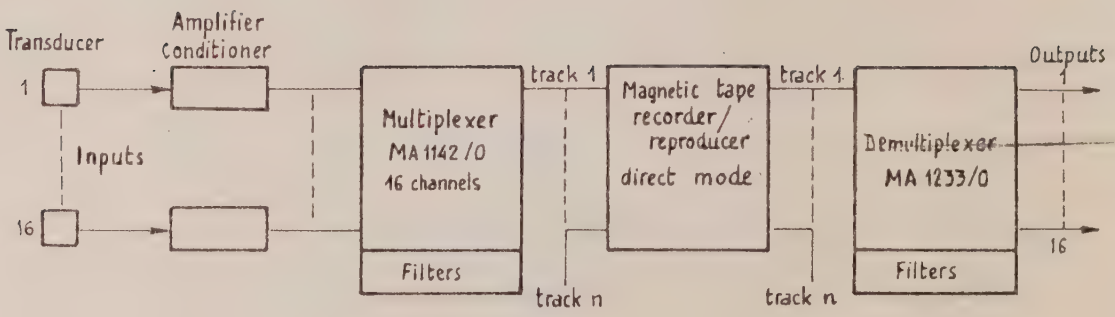


Fig.2 SCHEMATIC DIAGRAM

2 PREPARATION FOR USE - UTILIZATION

The record and read modules are defined at the time of order, by the following:

- Power supply voltage
- Inclusion of phase equalizer circuit or not
- Choice of record standard
- Connection of parameter input/output by terminal strip or multi-pin connector.

2.1 - Preparation for use

The record and read modules operate in association with a recorder equipped with Direct mode channels. All appropriate connections are assumed to have been made (see Operating Manual for each recorder).

.... - [illegible]

Connection is via the lead supplied with the modules (127 V or 220 V ± 10%). If no supply voltage is indicated in the order, the modules are prepared for 220 V operation. Line frequency can be 50, 60 or 400 Hz.

2.1.2 - Insertion of plug-in filter cards

Where record data bandwidth is known, the user inserts an input attenuator card in the record module. If record data includes harmonics the frequency of which is not known, filter cards are inserted in both record and read modules.

Filters are determined according to bit rate and number of channels (see table below). The same filters can be used for record and/or read.

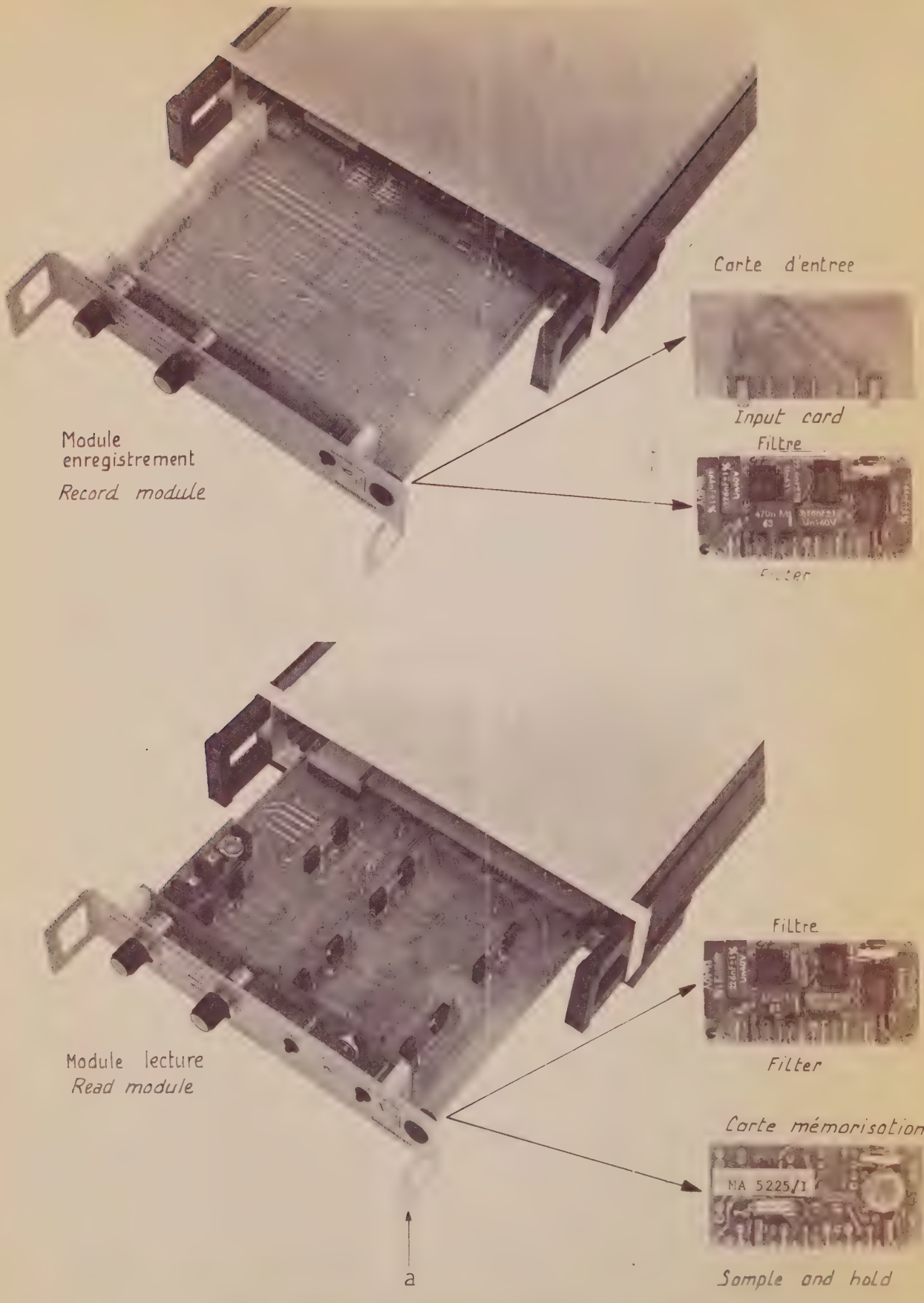


Fig. 3 - Modules Enregistrement et Lecture

RECORD AND READ MODULES

Min. Recorder bandwidth	Rate (kbit/s)	Bandwidth per channel				
		16 Channels	8 Channels	4 Channels	2 Channels	1 Channel
500 kHz	1000	2 kHz	4 kHz	8 kHz	16 kHz	32 kHz
250 kHz	500	1 kHz	2 kHz	4 kHz	8 kHz	16 kHz
125 kHz	250	500 Hz	1 kHz	2 kHz	4 kHz	8 kHz
62 kHz	125	250 Hz	500 Hz	1 kHz	2 kHz	4 kHz
31.2 kHz	62.5	125 Hz	250 Hz	500 Hz	1 kHz	2 kHz
15.6 kHz	31.2	60 Hz	125 Hz	250 Hz	500 Hz	1 kHz
7.8 kHz	15.6	30 Hz	60 Hz	125 Hz	250 Hz	500 Hz
3.9 kHz	7.8	15 Hz	30 Hz	60 Hz	125 Hz	250 Hz

The module must be opened to insert filter cards. For this purpose, pull the module out forwards, holding by the extractor handles (fig. 3, index a).

NOTE:

Always insert attenuator cards where filters are not used for record.

Unused inputs must be shorted, otherwise output voltage is not defined.

2.1.3 - Connection of parameters

Parameter connection can be by:

- Printed terminal strip
- 25-pin CANNON connector (see table below).

Connect the parameters to be recorded at the rear of module MA 1142/0 (CANNON connector) or MA 1142/1 (terminal strip).

Read signals are available on the rear panel of module MA 1233/0 (CANNON connector identical to that used for record) or MA 1233/1 (terminal strip).

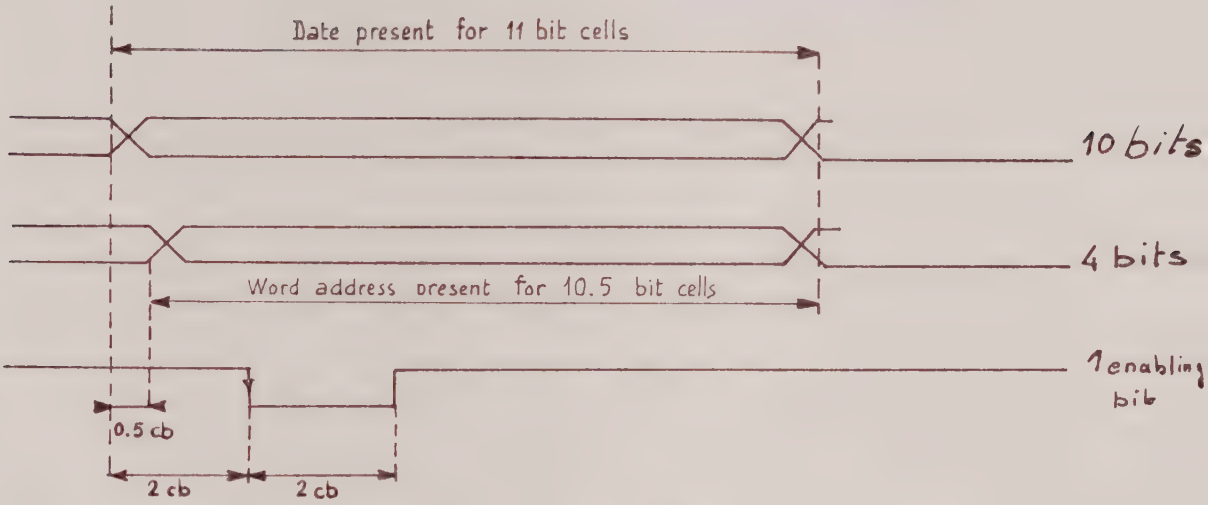
Pin No.	Function
1	Parameter 1
2	
3	Parameter 2
4	Parameter 3
5	
6	Parameter 4
7	Parameter 5
8	
9	Parameter 6
10	Parameter 7
11	
12	Parameter 8
13	Parameter 9
14	
15	Parameter 10
16	Parameter 11
17	
18	Parameter 12
19	Parameter 13
20	
21	Parameter 14
22	Parameter 15
23	
24	Parameter 16
25	Not connected

"Digital" connector (25-pin female)

Pin No.	Function
1	A (LSB word address code)
2	Bit 12 (LSB, 12-bit code)
3	11
4	10 (LSB, 10-bit code)
5	9
6	8
7	7
8	6
9	5
10	4
11	3
12	2
13	1 (MSB)
14	Not connected
15	MSG
16	[redacted]
17	Not connected
18	Not connected
19	Not connected
20	Sc (computer sync.: see following timing diagram)
21	Restored data output
22	Ho (0° clock: bit rate)
23	D } MSB
24	C } MSB word address code
25	B }

NOTE: TTL output logic, LS technology, fan-out 5 (LS).

MA 1233 DIGITAL OUTPUT TIMING DIAGRAM



(Signals shown for positive TTL)

2.1.4 - Selection of bit rate and number of input parameters

The desired values are chosen on two front panel selectors, marked "KB/S" and "ANALOG INPUT CHANNELS/ANALOG OUTPUT CHANNELS".

2.2 - Utilization

Having completed all connections, the modules are ready for immediate use, after switching on by depressing the MARCHE-ON pushbutton on the front panel.

The warm-up time for the associated magnetic tape recorder should be observed carefully.

Certain precautions are required for correct utilization of the equipment. In particular, check that:

- Parameter levels do not exceed ± 5 V, with impedance < 10 kΩ
- The associated recorder delivers an output level of 2.8 V pp (± 3 dB)
- The recorder is equipped with a phase equalizer (if not, see § 2.2.2.1).

2.2.1 - Selection of tape speed on associated recorder

The following table summarizes the different bandwidths of current Schlumberger recorders, together with details of record standard, number of parameters, and tape speeds.

2.2.2 - Checking correct operation of the complete system

The power supply lamps of both modules, together with the SYNC lamp should all be on.

If the SYNC lamp flashes, check:

- Correspondence between bit rate selection for record and read.

- Read signal drive level.

- Phase equalization:
  . If the recorder incorporates a phase equalizer, adjust equalization on the recorder.
  . If this is not the case, check that the phase equalizer is present on the module MA1233 printed circuit, and proceed as described below.

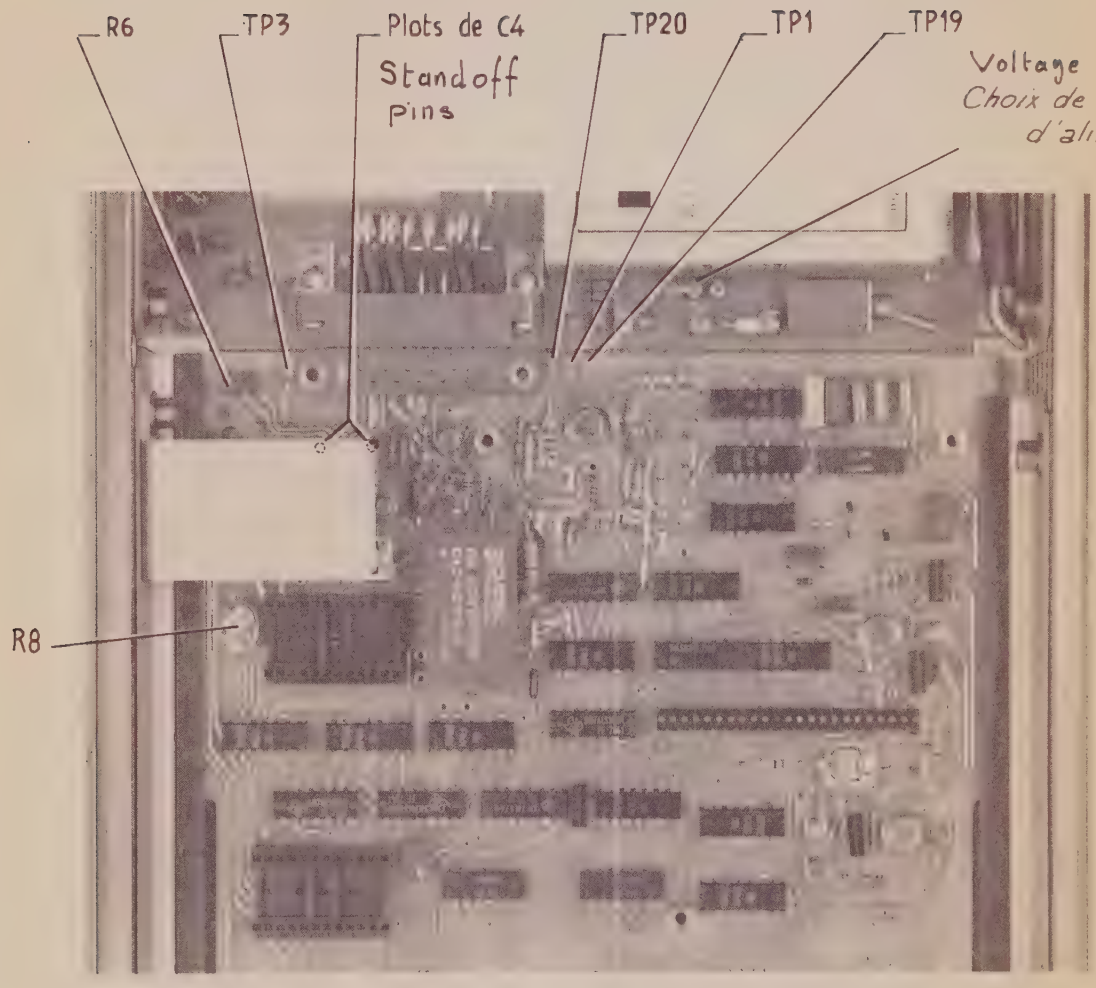


Fig. 4 - Correction de phase

Phase. équalization

2.2.2.1 - Adjustment of phase equalization for read module MA 1233 (see figure opposite)

Access to printed circuit

- Undo the two rear connector panel attachment screws (fig. 7, index a).

- Lower the connector panel.

- Slide out the upper protective cover.

- Disengage the flat cable.

- Solder capacitor C4, determined according to bit rate (see table below) to the contacts provided for this purpose.

Bit rate	Capacitor C4
1 Mb	330 pF mica 5% 63 V
500 kb	680 pF mica 5% 63 V
250 kb	1000 pF mica 5% 63 V
125 kb	2.2 nF polyester radial 400 V
62.5 kb	4.7 nf polyester radial 400 V
31.2 kb	10 nf polyester radial 250 V
15.6 kb	22 nf polyester radial 250 V
7.8 kb	47 nf polyester radial 100 V

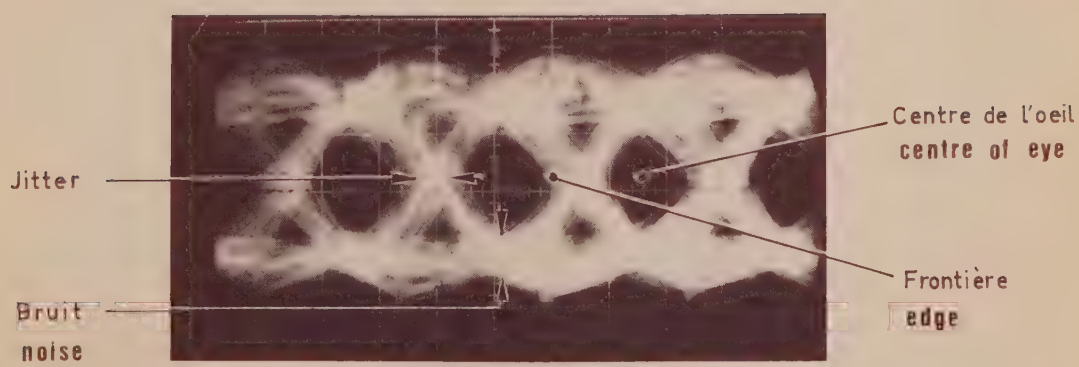


Fig.5 EYE_PATTERN ADJUSTMENT

Phase equalization is now optimum. Under these conditions, the SYNC lamp comes on.

Adjustment of phase correction (simplified procedure)

Proceed as follows for adjustment:

Equipment required: oscilloscope

- Connect pin 21 of the rear face digital connector to oscilloscope vertical amplifier input, triggering on "Ho" (output pin 22) and with ground on pin 16.

- Select an oscilloscope horizontal sweep rate giving 2 or 3 half-sine-wave parts.

- Adjust control R6 so as to obtain the largest possible central surface, with the blurred edges reaching as far as possible from the centre of the eye.

See eye pattern on page 2.9.

NOTE: Adjustment of phase equalization is only valid at the bit rate in question. When bit rate is changed, readjust after replacing capacitor C4 as appropriate.

2.3 Options

Various options can be indicated when ordering, these concerning:

- Power supply voltage
- Input level
- Output level
- Record standard (WBGI - WBGII)
- The phase equalizer described above.

These options can be implemented by the customer, corresponding procedure being as follows:

2.3.1 - Modification of power supply voltage (modules MA1142 and MA1233)

Position the jumper according to desired power supply voltage: 127 V or 220 V. Execute this modification on both modules (see fig. 4).

2.3.2 - Adjustment of MA1142 input sensitivity

Unless otherwise specified at the time of order, the MA1142 module is set for $\pm$ 1 V input sensitivity.

Proceed as follows if modification is required:

1) Open module MA1142 (see paragraph 2.1.2).
2) Referring to the attached arrangement diagram, remove straps ST3 - ST4 - ST5 and ST2.
3) Connect the straps as indicated in the following table, according to input level.

Input level	Straps
± 5 V	ST3 - ST6
± 2.5 V	ST2 - ST6 - ST4
± 1 V	ST2 - ST6 - ST5

NOTE: Settings for unbalanced input voltages (0/+2 V or 0/+5 V) require readjustment of the ADC. The user is not advised to undertake this conversion himself.

2.3.3 - Adjustment of MA1233 output level

Unless otherwise specified at the time of order, the MA1233 is adjusted for an output voltage of ± 1 V. Settings for other output levels (± 2.5 V or ± 5 V) require readjustment of the DAC. It is not advisable for the user to undertake this conversion himself.

2.3.4 - Conversion for 12-bit operation

This modification requires readjustment of the ADC on the MA1142, and the VAC on the MA1233. It is not advisable for the user to undertake this conversion himself.

CHAPTER III

DESCRIPTION

Fig. 6 - FRONT VIEWS - Record module
- Read module

Fig. 7 - REAR VIEWS - Record module
- Read module

Fig. 8 - INTERNAL VIEWS - Record module
- Read module

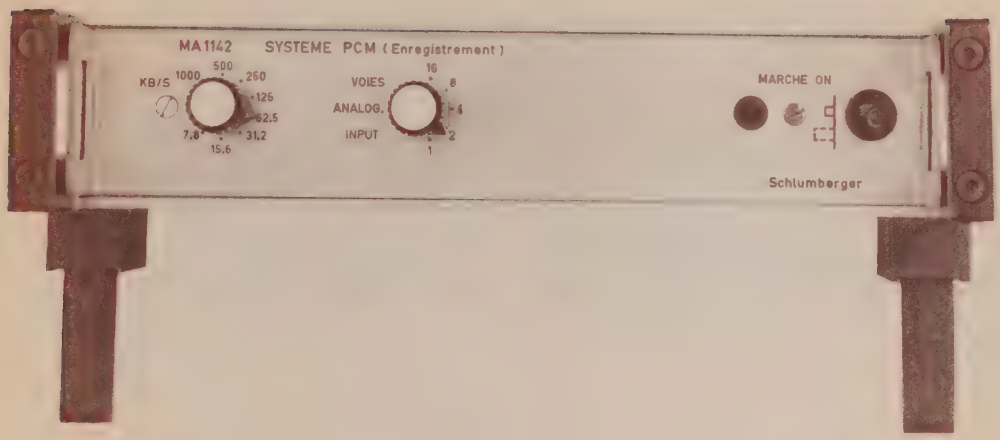
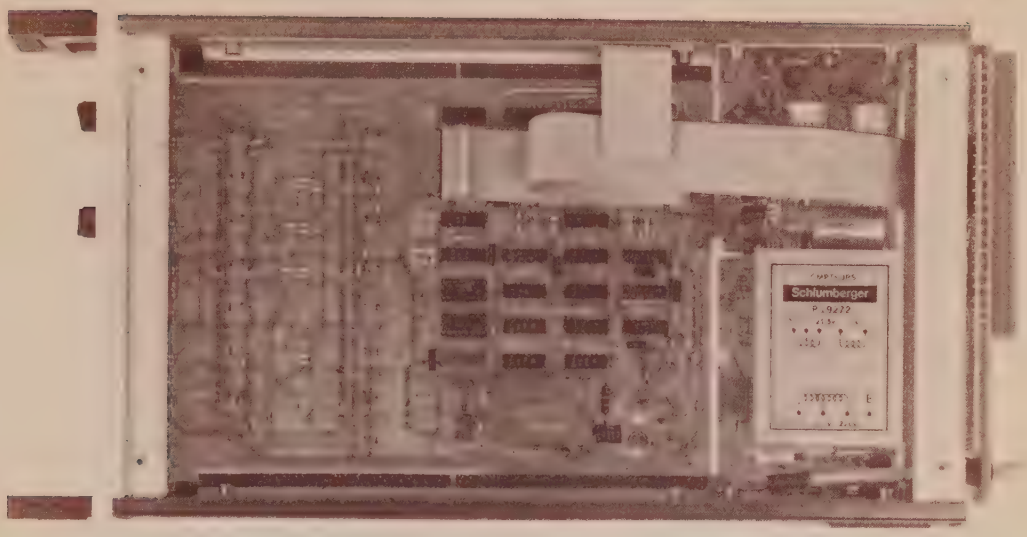


Fig.6. Vues avant

Fig.7. Vues arrière

REAR VIEWS



Module Enregistrement
Record module

Module Lecture
Read module

Fig. 8 - Vues intérieures

INTERNAL VIEWS

CHAPTER IV

OPERATION

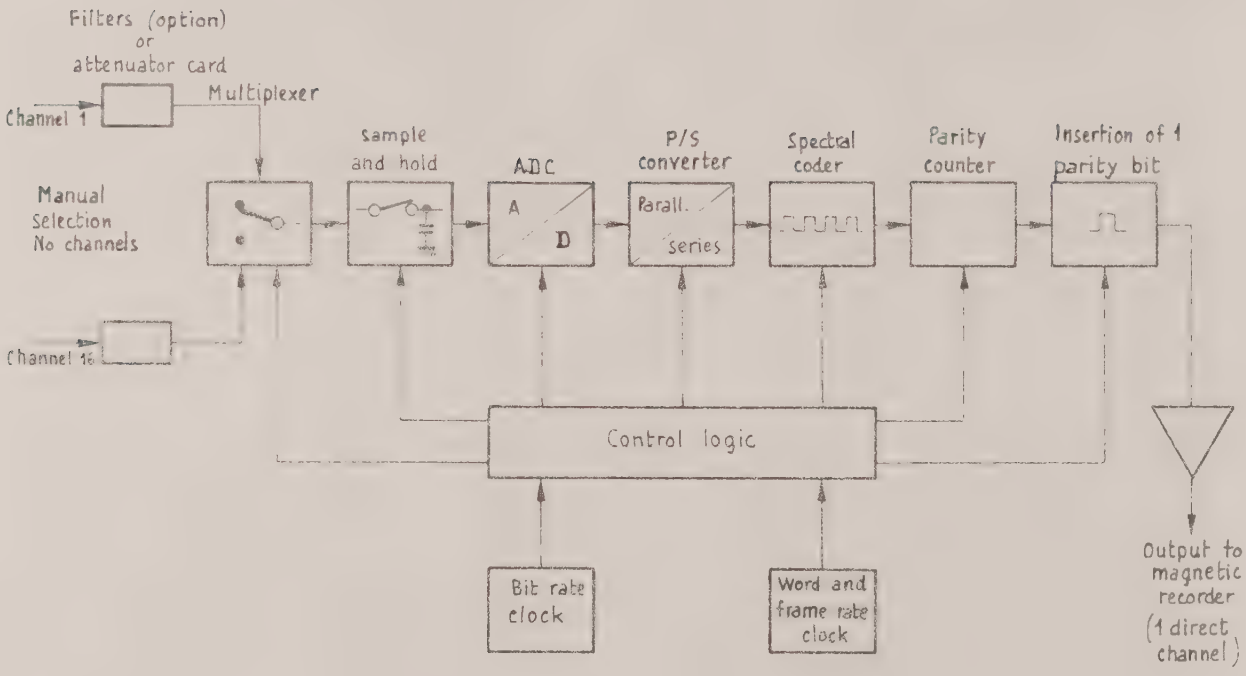


Fig. 9 RECORD FUNCTION BLOCK DIAGRAM

4.1 - RECORD LOGIC CARD

Type MA 1142/0 (terminal strip connection)

MA 1142/1 (multi-pin connector).

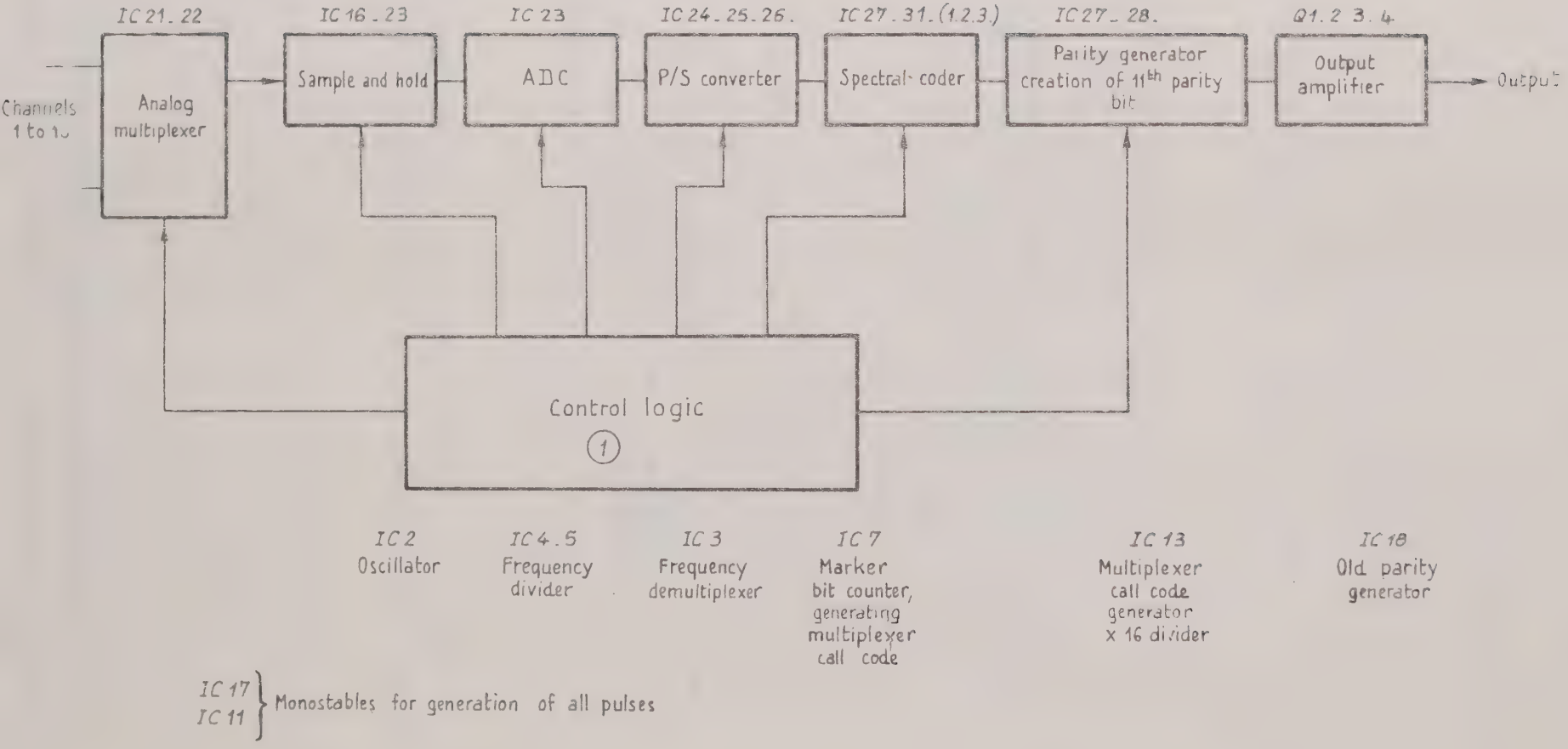
This card comprises a control logic block for the various stages.

Control logic

This includes a 2 MHz oscillator, comprising circuit IC2 and crystal Y1, followed by circuits IC4 and IC5, forming a x2 divider chain. Type 74151 logic demultiplexer IC3, driven by a 3-bit address code inputting on pins 9, 10 and 11 respectively, is used to select the correct bit rate. The address code is generated on the "service" card, by diode matrices CR1 to CR11, and integrated circuit IC1 on the logic card. Bit rate clock Ho appears on TP1, at output of integrated circuit IC3. This clock drives a "marker bit" circuit, generating the word rate. This comprises shift registers IC7 and IC8, diodes CR1 to CR12, and integrated circuit IC6. This assembly generates one pulse every 11 clock bits. This pulse, $\overline{CM}$, appears on TP9. The word rate clock drives a x16 divider, comprising integrated circuit IC13, which generates the input multiplexer 4-bit call code. Monostable circuits IC17 and IC11 generate pulses driving, respectively, the multiplexer, sample-and-hold, ADC and "scrambling" circuit. These pulses are designated $\overline{dCM}$, $\overline{dHo}$, dCM, ddCM, on the diagram.

We therefore have bit rate Ho (TP1), word rate $\overline{CM}$ (TP9), input multiplexer addressing code, and the various record logic command pulses.

The 16 analog input parameters are multiplexed in circuits IC21 and IC22, each comprising an 8-channel multiplexer driven by a 4-bit code generated by IC13 (described above). Each sample taken is applied to sample-and-hold IC13, the function of which is to hold the parameter constant at detected value, for approx. 6 µs. This time is required by the ADC to execute its function. Holding of the sample in IC13 is controlled by the "status" position (pin 20 of IC23) of the ADC. Converter output is on 10 parallel bits, representing the sample converted into digital form. The 10 bits are stored in three


IC 21. 22
IC 16. 23
IC 23
IC 24. 25. 26.
IC 27. 31. (1.2.3.)
IC 27. 28.
Q1. 2 3. 4
Channels 1 to 16
Analog multiplexer
Sample and hold
ADC
P/S converter
Spectral coder
Parity generator creation of 11th parity bit
Output amplifier
Output
Control logic
(1)
IC 2
Oscillator
IC 4. 5
Frequency divider
IC 3
Frequency demultiplexer
IC 7
Marker bit counter, generating multiplexer call code
IC 13
Multiplexer call code generator x 16 divider
IC 18
Old parity generator
IC 17
IC 11
Monostables for generation of all pulses

shift registers (parallel input/series output type), IC24, IC25 and IC26, register advance being driven by clock Ho with hold-off on bit 11. The data, available in series form on TP13, is then scrambled by circuits IC27 and IC31. IC27 and flip-flop IC28 calculate the parity of the 10 scrambled bits. This parity, available on pin 5 of IC28, is present every 10 bits. The parity bit is included in the data as bit 11, so as to create a PCM word comprising 10 data bits and 1 parity bit.

The 10 bits of spectrally coded data are transferred by gate IC12, and are available on TP14 ($\overline{CM}$ = "1" and CM = "0", for the first 10 bits). On appearance of bit 11, $\overline{CM}$ changes to "0" and CM changes to "1", transferring the previously calculated parity bit to TP14. On the 16th word, a "1" appears on pin 9 of IC27, inverting calculated parity. The odd parity bit is then transferred to TP14, this identification bit eliminating frame ambiguity on read.

Flip-flop IC28, on output 3 of IC12, provides phase-alignment of data and clock. The circuit comprising transistors Q1, Q2 and Q3 delivers the data at an impedance of 50 Ω, with an output level adjustable between 0 V and 10 V pp (standard level: 2.8 V pp).

Resistors R41, R42, R38, R36 and R35 programme the sample-and-hold for different input voltages:

- Standard: $\pm$ 1 V
- Options: $\pm$ 2.5 V, $\pm$ 5 V, 0/+2 V or 0/+5 V.

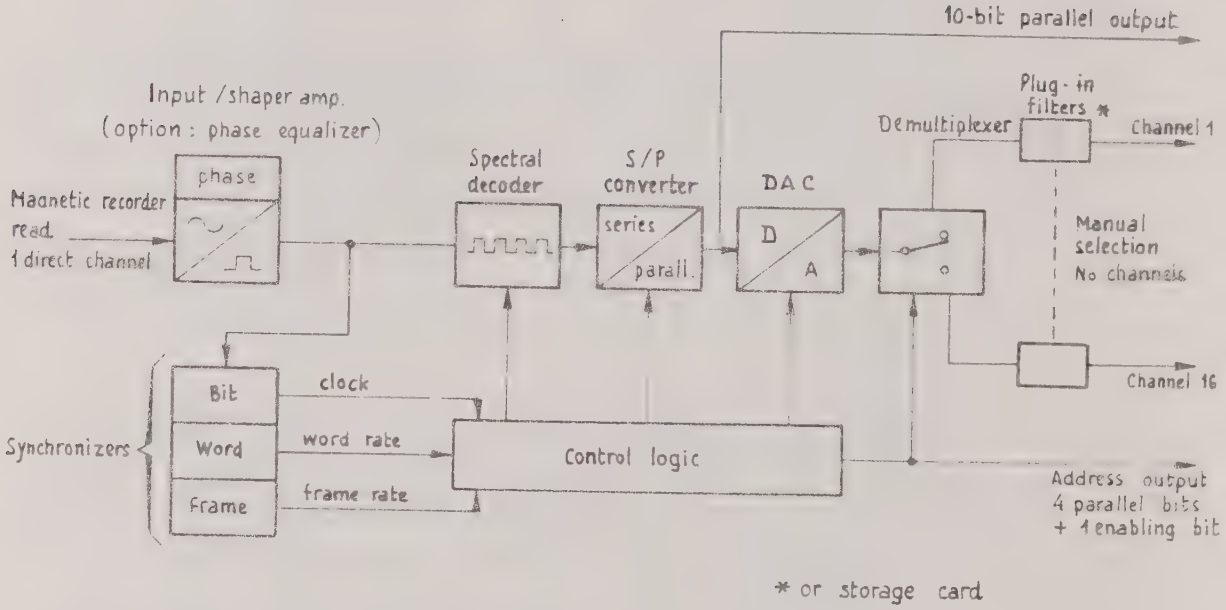


Fig. 11 READ FUNCTION BLOCK DIAGRAM

4.2 - READ LOGIC CARD

Type MA 1233/0 (terminal strip)
MA 1233/1 (multi-pin connector)

PCM data is applied to transistor Q1, via capacitors C1 and C2 (cross-coupled to eliminate the influence of polarity). Transistor Q1 is used in the common collector mode, and data outputs on the emitter of Q1 at low impedance.

A phase equalizer circuit, comprising Q1, C4, R6, R7 and R8, is wired on the card. However, this device is an option, and the user must connect capacitor C4 according to selected bit rate. The processed data is applied to Q3, used in the common collector mode, which drives a DC component restoration circuit, comprising C1, R10, R15, R16, R17, R21 and C11 or C8, the function of which is to hold constant the levels differentiated by the recorder channel. The data is then applied to one input of comparator IC1 (input 3), the other input receiving the reference, namely the data attenuated by the ratio of R16 (MSG - 5 V). As a result, the baseline decreases in the same way as the data.

A delay is introduced on the positive or negative transitions, by means of filter R16 + R10 or C11, so that the baseline passes in the opposite direction to the data. The restored data is available on output of the comparator circuit, in TTL level form for driving the control logic, synchronizers, and processing stages.

4.2.1 - Bit synchronization

The bit synchronizer is used to restore the clock, it comprises:

Phase comparator IC15, IC4, IC43, IC21, and resistors R45 to R51, which generate a voltage proportional to the phase difference between the data, and clock "Ho" restored by the VCO. This output drives circuit IC20, which amplifies phase comparator output with a predetermined gain. This voltage is

then filtered by R37 and R38, and capacitors selected from C15 to C24 according to bit rate, by 3-bit code A - B - C appearing on pins 9, 10 and 11 of analog demultiplexer IC17.

Output voltage from operational amplifier IC20, after amplification and filtering, drives VCO circuit IC19, Q6, R31, R26, R32, R33, C33, C36, CR8 and R6. IC19 is an operational amplifier, triggered at a hysteresis value representing a certain fraction of output voltage applied to input. This ratio is determined by R26 and R31. Capacitor C33 is charged by transistor Q6 at constant current. By varying the emitter voltage of this transistor, current modulation is produced at output of IC19, with resultant frequency modulation. Diode CR8 and capacitor C26 compensate temperature drift, and increase transition rapidity. Clock "2 Ho" is available on TP14. This signal is then divided by 2 by circuit IC18.

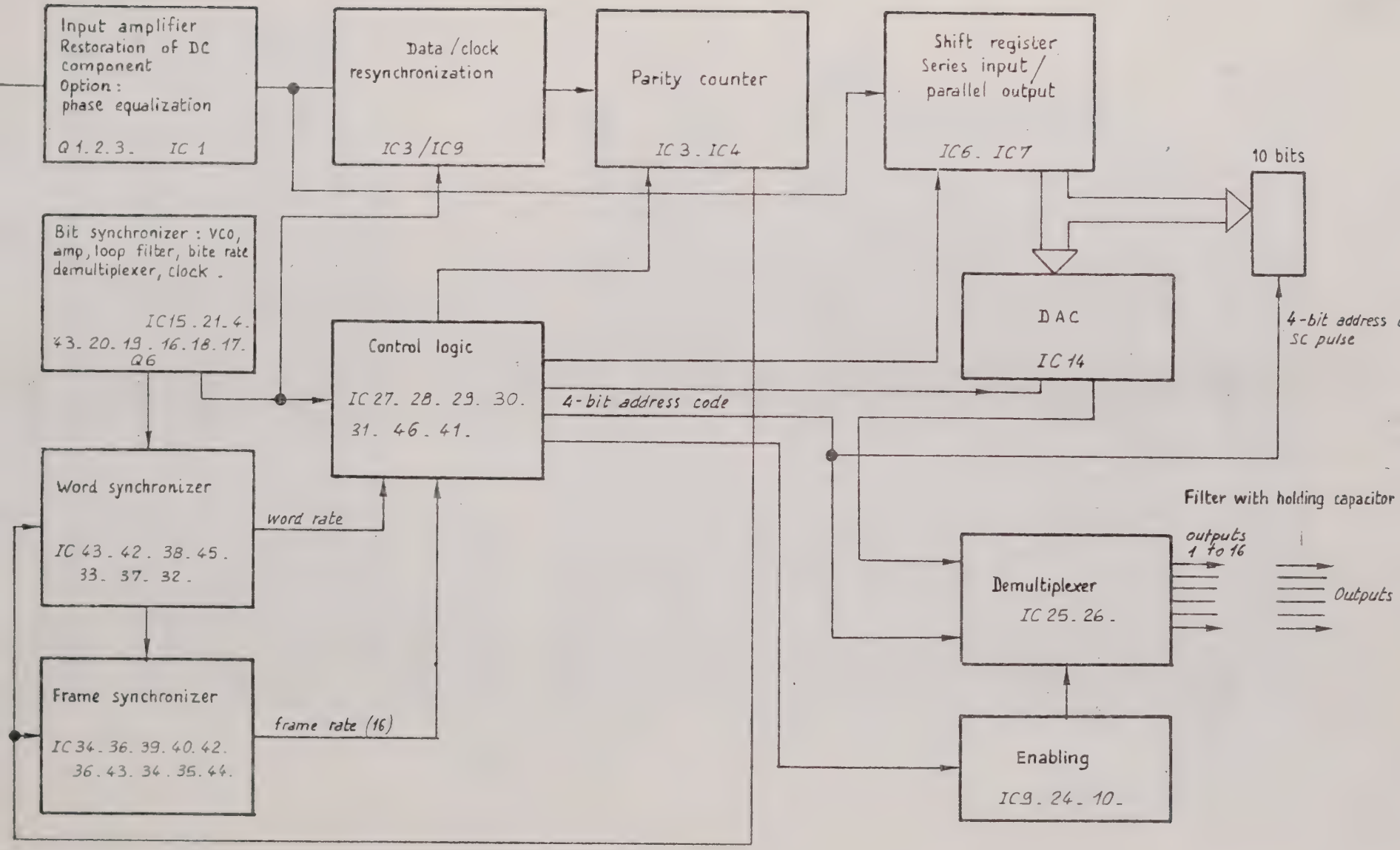
Digital demultiplexer IC16 is used to select correct bit rate, using address code A - B - C and divider chain IC18. $\overline{Ho}$ is obtained at demultiplexer output, on pin 5 of IC16. Circuit IC2 inverts clock $\overline{Ho}$, and the clock signal is therefore restored at bit rate.

4.2.2 - Word synchronizer

. Principle

We have seen that the PCM frame comprises 16 words of 11 bits. Each word corresponds to 10 data bits coded spectrally, and one parity bit resulting from calculation of the 10 preceding bits. The particularity of this frame is to be found in the 16th word, in which bit 11 is no longer the parity bit, but an odd parity bit. This means that calculation results give a logic "1" for the first 15 words, and a "0" for the 16th word. The result appears systematically for every 11 bits, throughout the frame.

The data is coded spectrally, giving an occurrence probability of 1/2 for "0" and "1" bits.


Input amplifier
Restoration of DC component
Option :
phase equalization
Q 1. 2. 3. IC 1
Data / clock resynchronization
IC 3 / IC 9
Parity counter
IC 3 . IC 4
Shift register
Series input / parallel output
IC 6 . IC 7
10 bits
Bit synchronizer : VCO, amp, loop filter, bite rate demultiplexer, clock .
IC 15 . 21 . 4 . 43 . 20 . 19 . 16 . 18 . 17 . Q 6
Control logic
IC 27. 28. 29. 30. 31. 46. 41.
DAC
IC 14
4-bit address code
4-bit address
SC pulse
Word synchronizer
IC 43 . 42 . 38 . 45 . 33 . 37 . 32 .
word rate
Filter with holding capacitor
outputs 1 to 16
Demultiplexer
IC 25 . 26 .
Outputs
Frame synchronizer
IC 34 . 36 . 39 . 40 . 42 . 36 . 43 . 34 . 35 . 44 .
frame rate (16)
Enabling
IC 9 . 24 . 10 .

In the calculation executed every [illegible] bits of the frame, occurrence probability for a logic "1" is 15/16 or [illegible].

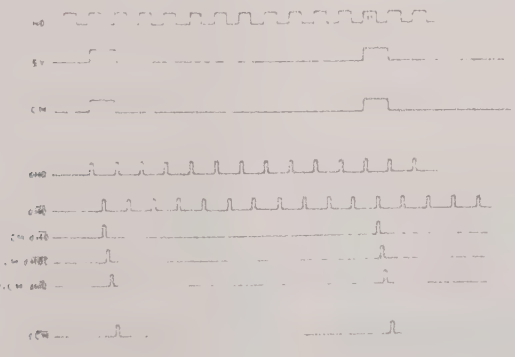
Start of parity calculation sequence for the 11th bit can be on any bit of the data. If the result of this calculation is a logic "1", the circuit records this correct result by incrementing an up/down counter by one unit. If the result is a "0", the counter is decremented by two units. A statistical check is therefore made on two probabilities: P1 = 15/16 and P2 = 1/2 x 2 or 1/4. On each bad result, the pointer indicating start of calculation advances by one step, pointer state remaining unchanged if the result is positive. After a number of frames, the system eliminates word ambiguity, confirming a CM word rate pulse, when the modulo 16 up/down counter shows 8.

. Master

Clock Ho, restored by the bit synchronizer, triggers a monostable generating pulse $\overline{dHo}$, which increments modulo 11 marker bit counter IC30, IC31, IC46, CR11, CR22. Counter output delivers a CM pulse every 11 bits. The word synchronization pulse is available on TP8. This pulse increments modulo 16 counter IC34, which generates the 4-bit demultiplexer address code.

Logic block IC27, IC28, IC29, IC10-4 delivers the pulses required for operation of this assembly: $\overline{dHo}$, CM.$\overline{dHo}$, CM.$\overline{dHoC}$, d(CM - $\overline{dHo}$), and $\overline{dCM}$ (see timing diagram below):

TIMING DIAGRAM



The circuit calculating bit 11 parity comprises IC3/1, IC3/2 and IC4/1. The result of this calculation, SY, is available on pin 3 of IC3/2. Pulse $\overline{d(CM.\ d\ \overline{Ho})}$, indicating start of calculation, resets the parity counter every 11 bits (pin 13 of IC3/2).

Every 11 bits, calculation result SY is examined inside scan window CM . d $\overline{Ho}$. If a "1" is present, circuit IC33 (modulo 16 up/down counter) is incremented by one unit on input 5. If the result is a "0", IC33 is decremented by 2 units, by application of pulses CM d $\overline{Ho}$ and CM d Ho C on decremental input 4. When the result is "bad", the word counter is advanced by one step, by applying pulse $\overline{CM\ d\ \overline{Ho}}$ to pin 1 of IC43, corresponding to displacement of the start of calculation pointer by one unit.

When counter IC33 $\geq$ 8 (DI = 1), word rate is confirmed by inhibiting IC37/1, which displaces the pointer. An enabling flip-flop generates a "1" on pin 9 of IC32/2, indicating that ambiguity has been eliminated.

The system is no longer in the search mode, and the counter stops at 16. When the counter again goes below 8 during operation, the system restarts in the search mode. It is therefore necessary to "lose" 4 words to disrupt synchronization.

. Elimination of frame ambiguity

The same procedure is used as for word ambiguity, utilizing pulses SY and $\overline{SY}$. The reference is a "0" appearing every 16 words, namely on calculation of odd parity. Pulses are counted in up/down counter IC35, via CC16.

The scanning window is placed on the 16th word, $\overline{SY}$ is taken as the reference, and scanning occurs in the interval CM $\overline{d\ Ho}$. If the result is positive, the counter is incremented, or decremented for a negative result. Address counter IC34 is incremented by 1, by applying pulse $\overline{d(CM.d\overline{Ho})CC16}$ to pin 12 of IC43. The counter is a x16 divider, generating the 4-bit

A - B - C - D address code for the demultiplexer circuit. CC16, determined by IC39, represents the frame synchronization pulse. When CC16 is detected, enabling flip-flops IC32/1 and IC44 are locked.

Pulse W is available on pin 6 of IC44, and bit rate Ho, word rate CM and frame rate CC16 are thus restored.

The data available on pin 7 of IC1, restored in TTL level form, is applied to input of the descrambling circuit comprising IC4 and IC5. The decoded message is sent to 10-bit shift register IC6 - IC7, with series input and parallel output. The 10 data bits are applied to storage circuit IC8 - IC11 - IC12. At a certain moment of d $\overline{CM}$, the status of shift register IC6 - IC7, namely a special 10-bit word, is stored in these circuits. This word, converted to analog form, is available on pins 15 and 18 of IC14. The data is sent to input 3 of demultiplexer IC25 - IC26. Address code A - B - C - D selects the correct channel number, and drives demultiplexer IC9 - IC24 - IC10, as long as elimination of word rate CM ambiguity has not enabled flip-flop IC9, output Q1 of flip-flop IC44 being at "0". On elimination of ambiguity, the flip-flop changes to "1", releasing the system on the following pulse.

Circuit IC41/2 gives intersection between W and frame ambiguity elimination D2 and C2, cancelling hold-off on flip-flop IC9 and enabling demultiplexer IC26 - IC25.

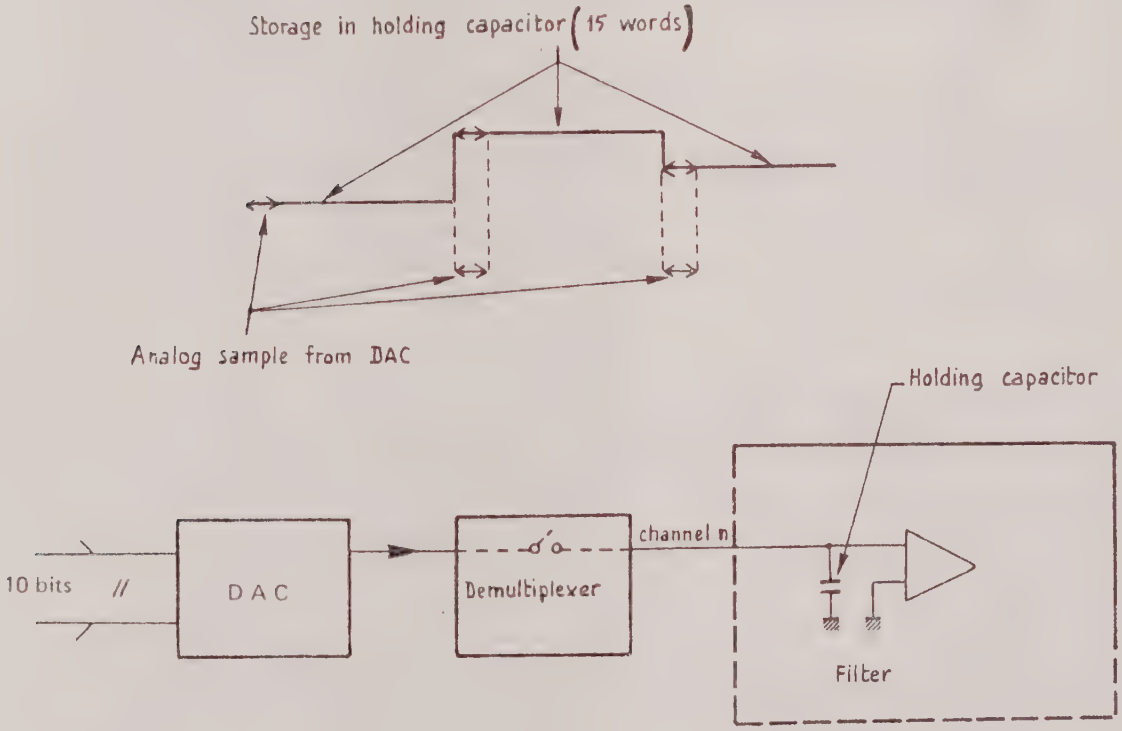
Channels 1 to 16 are available at demultiplexer output, on one of outputs 13, 14, 15, 12, 1, 5, 2 or 4 of IC25 - IC26. These drive the holding capacitor (storing all analog data), on each (optional) filter. The 10 data bits accompanied by the 4 address bits, are available on the rear panel "digital" connector. These 10 bits are picked off directly from the digital input of the converter, pins 1 to 12 of IC14. The 4 address bits, A - B - C - D, are picked off in parallel at demultiplexer input. Also available on this connector are the data, restored in TTL level form, restored clock Ho, and pulse SC authorizing computer acceptance of all data.

The SYNC lamp on the front panel of the unit, comes on to indicate that the system is fully synchronized (bit, word and frame

synchronization), and that the unit is operational.

4.3 - RECOVERY FILTER

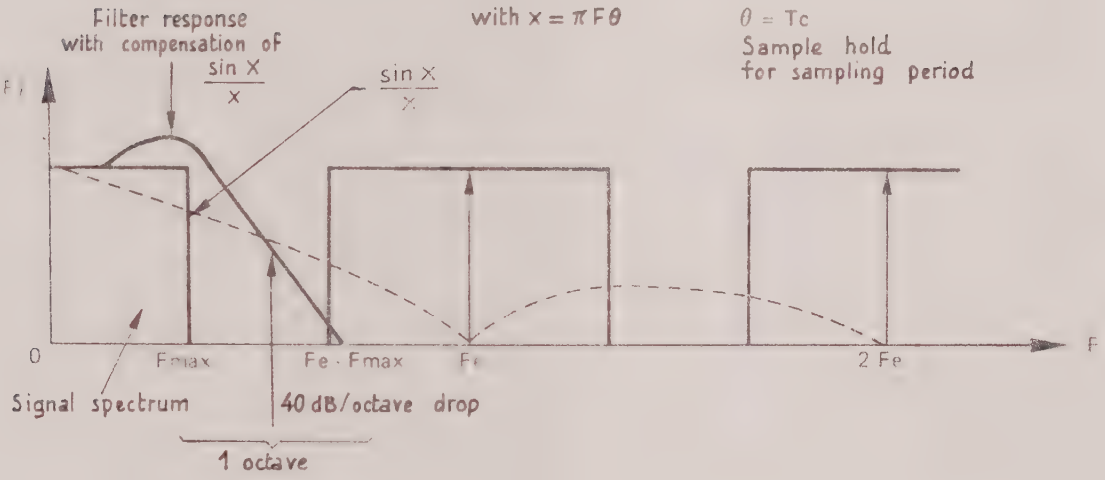
Digital/analog converter IC14 converts each 10-bit word present at input, into analog sample form. Each sample is selected, and sent to the correct channel by demultiplexer IC25 - IC26. Sample time is equal to 1 word (10-bit output). Each sample must therefore be stored throughout the remainder of the frame (15 words) in a holding capacitor, as shown in the figure below:



This principle involves the use of 1 storage capacitor per channel. This capacitor is calculated according to selected bit rate, and is the result of a compromise between rapid charge and a holding tolerance of 0.001 during storage. These considerations have led to the capacitor being wired to the recovery filters.

The demultiplexer and holding capacitor form a sample-and-hol .

Restoration of the signal in analog form requires frequency filtering in the 0 - F max. band (see figure).



The filter used is of the 5th order Tchebyscheff type, with Sallen Key structural modification. The response curve of this filter shows an increase from frequency F max./2 up to F max., so as to compensate the $\frac{\sin x}{x}$ term resulting from sampling with hold. At F max., the curve decreases as a slope of 40 dB/octave. At 2 F max., attenuation is 1/100. This results in residual spurious modulation of about 1/100 at F max., by the periodized and offset spectrum of the data centered on 1 Fc.

The filter card comprises 3 stages:

- The first stage comprises the holding capacitor, followed by operational amplifier IC1, giving very high input impedance ($Zin \geq 10^8$ Ω). Discharge of capacitor C6 during the holding phase is therefore very low.

- The other two stages form the filter proper.

The first filter stage, comprising IC2, R3, R1, R2, C3, C2, C1 has an overvoltage factor of 3.22.

The global transfer function for these two cells synthesizes the response of the recovery filter previously described.

The restored signal is available in analog form on pin 6 of IC3, at an output impedance $\leq$ 2.5 Ω, with max. admissible output 5 mA.

Factory-adjusted control R6 cancels out spurious offset voltage for the complete filter.

The filters can be used both for record and/or read. Storage capacitor IC6 is cut in automatically for read, by grounding pin SH. However for record, this pin is open-ended, and the holding capacitor is cut out. When filters are used for both record and read, a compromise is adapted for the channel determining optimum tolerance, namely:

- Complete system with record module, read module and recovery filter:

  + 0.5 dB, - 1 dB

- Complete system with record module and filter, read module and recovery filter:

  + 1.5 dB, - 1 dB.

These values go up to cut-off frequency Fmax.

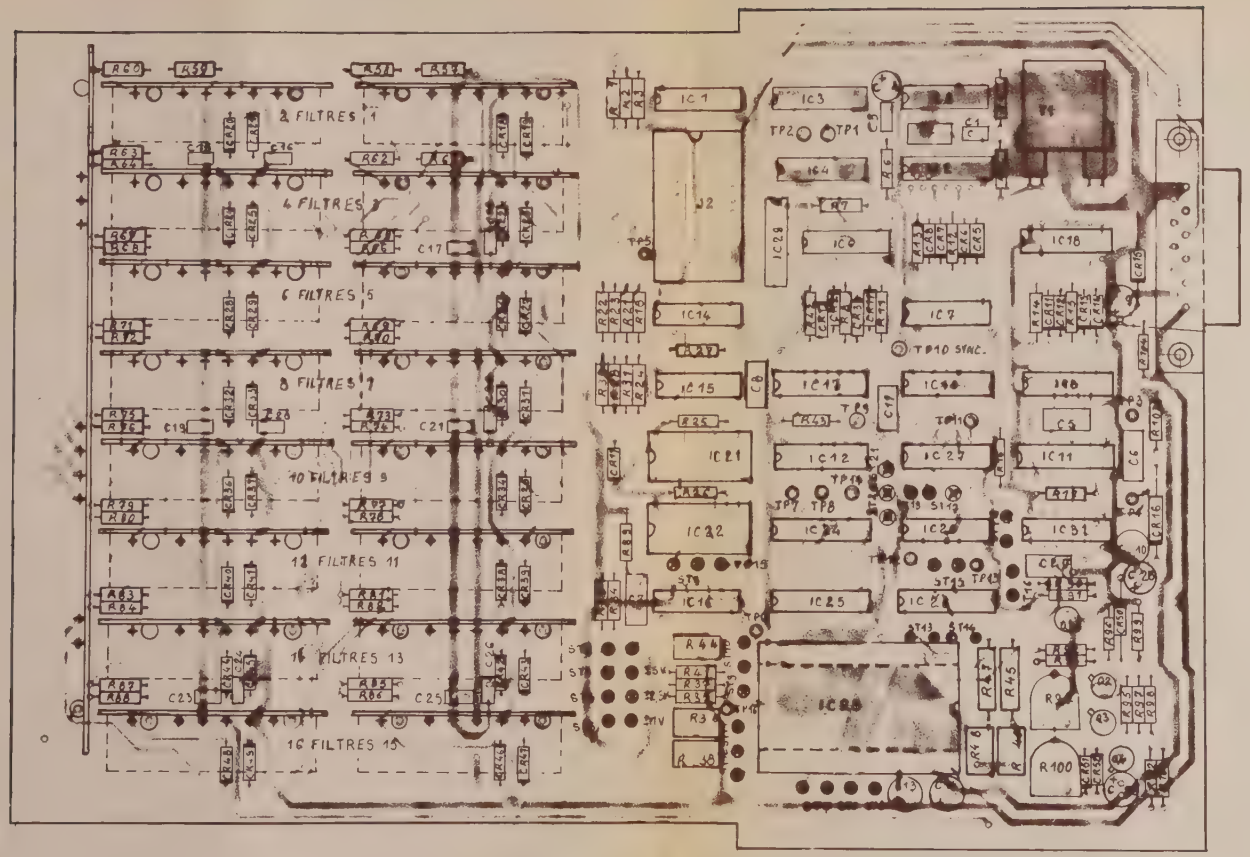
These filters have marked group differential distortion, which means that transients are slightly distorted, this being the case for a square-wave signal.

The multiplexing principle does not produce an inherent phase differential lag. As a result, distortion introduced by the filters has no influence on digital output (distortion approx. $\pm$ 10° between two filters at cut-off frequency). Each filter is defined for a given bit rate and number of channels. Selection of these two parameters by the user therefore determines bandwidth and filter.

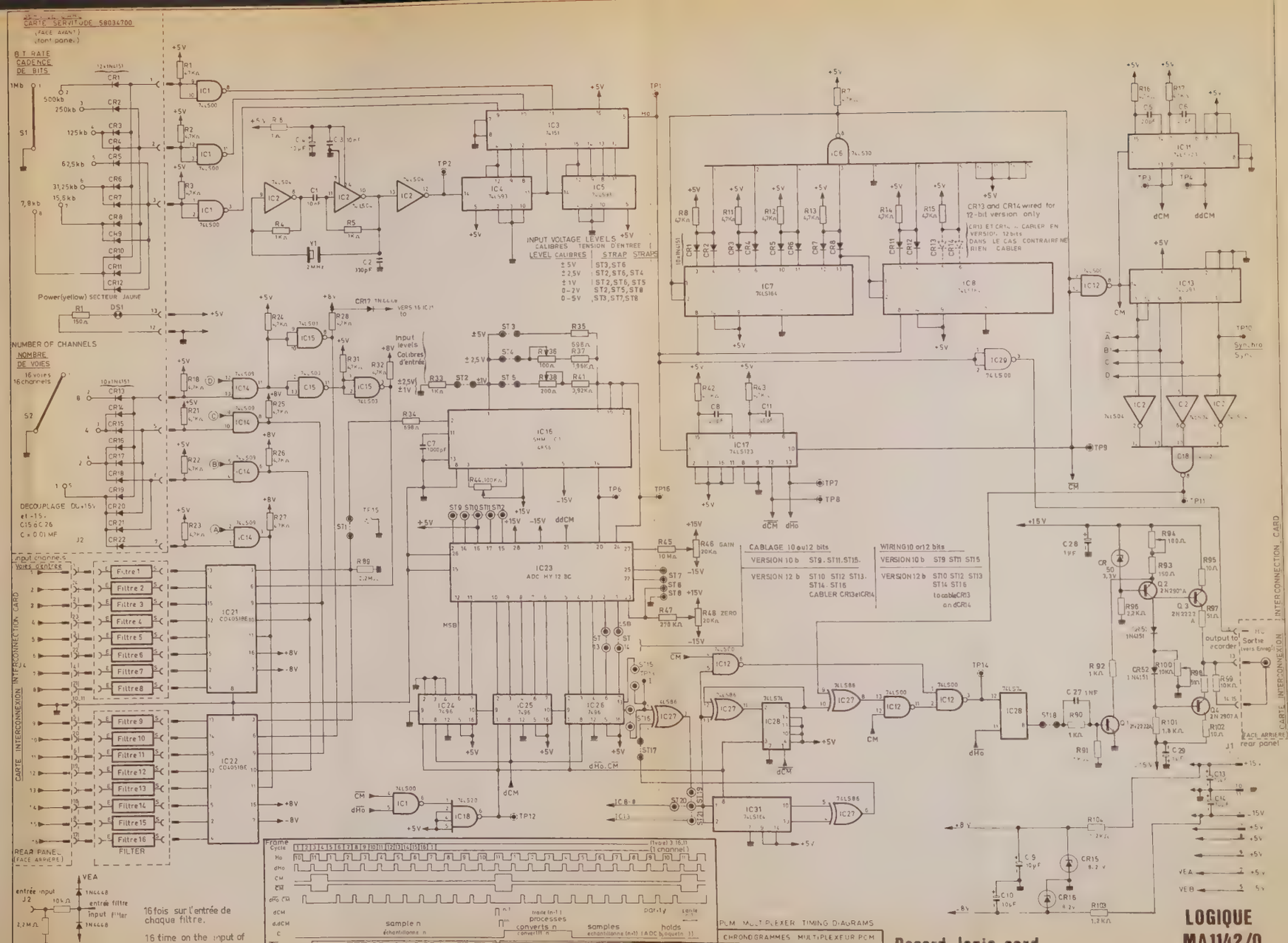
4.4 - STORAGE CARD

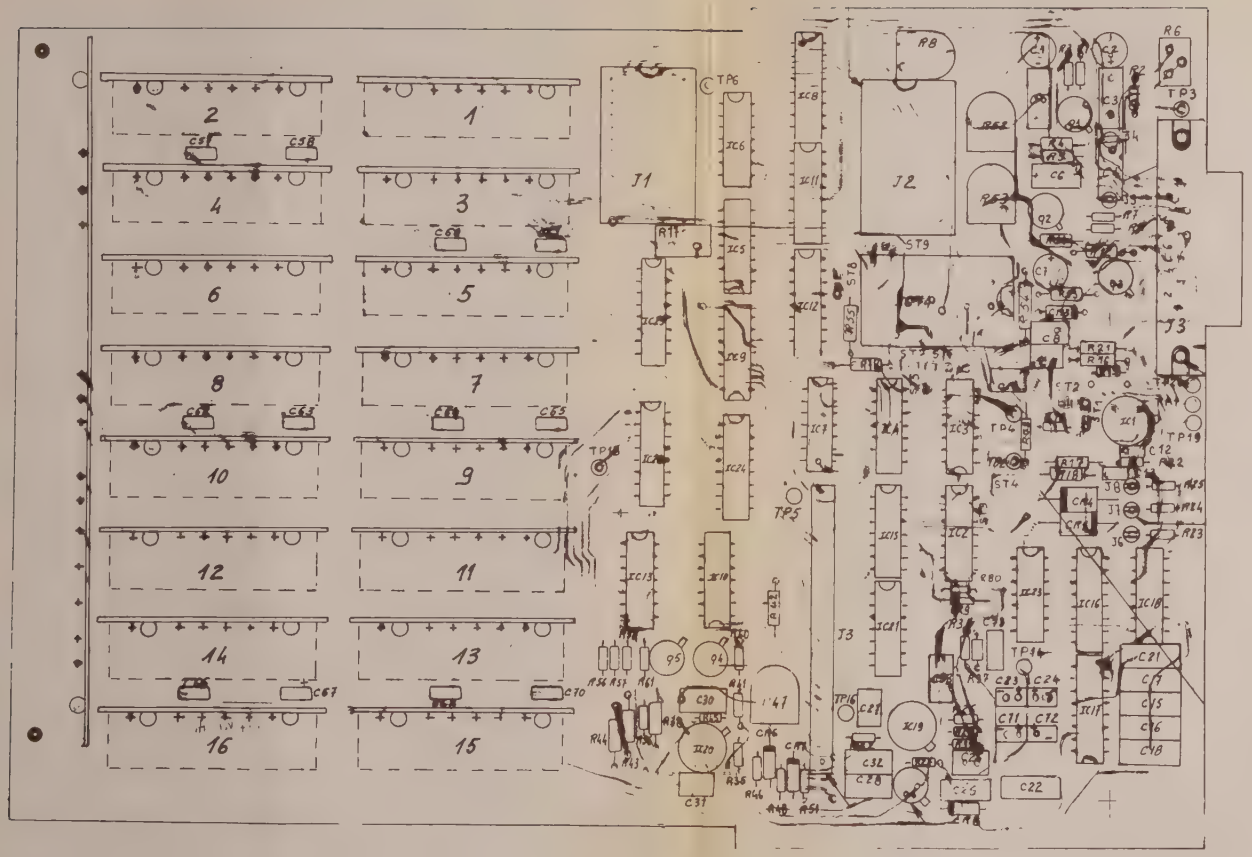
This card is used at demultiplexer output in place of the filter, to restore an unsmoothed sample signal. In this case, the smoothing function is provided by the user, as required.

This card incorporates a storage capacitor, and an operational amplifier for impedance matching (high input impedance and low output impedance).

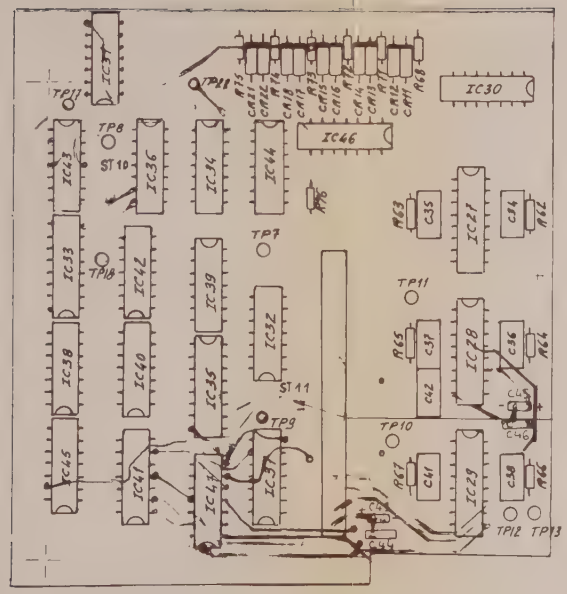


Record logic card
CARTE LOGIQUE ENR!

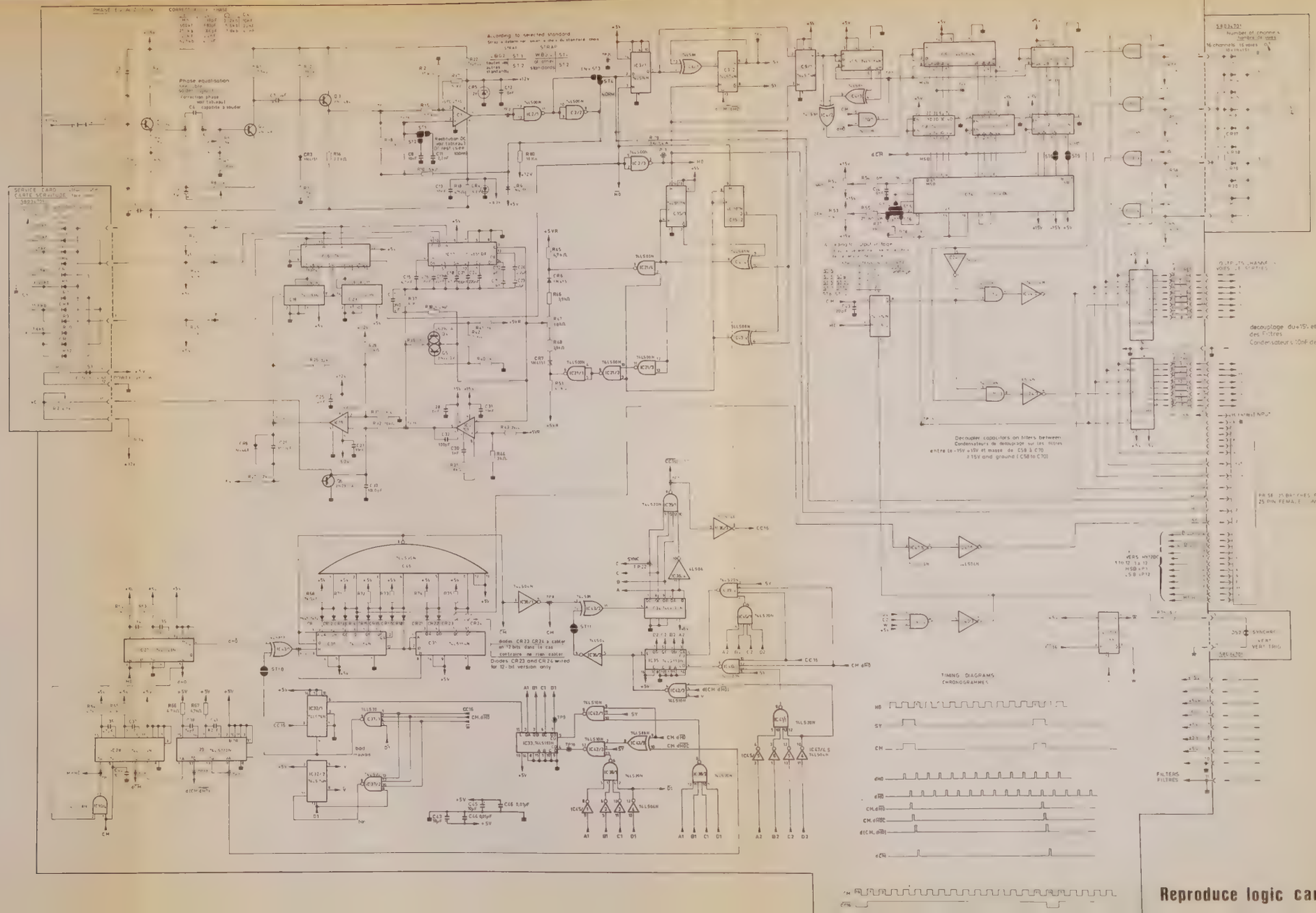

CARTE SERVITUDE 58034700
(FACE AVANT)
(front panel)
BIT RATE
CADENCE
DE BITS
1Mb
500kb
250kb
125kb
62,5kb
31,25kb
15,6kb
7,8kb
S1
Power(yellow) SECTEUR JAUNE
NUMBER OF CHANNELS
NOMBRE
DE VOIES
16 voies
16channels
S2
DECOUPLAGE DL+15V
et -15V
C15 à C 26
C = 0.01 MF
J2
CARTE INTERCONNEXION INTERCONNECTION CARD
Input channels
Voies d'entrée
Extre 1
Filtre 2
Filtre 3
Filtre 4
Filtre 5
Filtre 6
Filtre 7
Filtre 8
Filtre 9
Filtre 10
Filtre 11
Filtre 12
Filtre 13
Filtre 14
Filtre 15
Filtre 16
FILTER
REAR PANEL
(FACE ARRIERE)
entrée input
J2
10kΩ
2,2MΩ
entrée filtre
input filter
1N4448
VEA
16 fois sur l'entrée de chaque filtre.
16 time on the input of
INPUT VOLTAGE LEVELS
CALIBRES TENSION D'ENTREE
LEVEL CALIBRES
STRAP STRAPS
±5V ST3,ST6
±2,5V ST2,ST6,ST4
±1V ST2,ST6,ST5
0-2V ST2,ST5,ST8
0-5V ST3,ST7,ST8
CR13 and CR14 wired for 12-bit version only
CR13 ET CR14 A CABLER EN VERSION 12 bits DANS LE CAS CONTRAIRE NE RIEN CABLER
CABLAGE 10 ou12 bits
VERSION 10 b ST9 . ST11.ST15.
VERSION 12 b ST10 ST12 ST13. ST14 ST16 CABLER CR13etCR14
WIRING10 or12 bits
VERSION10 b ST9 ST11 ST15
VERSION12 b ST10 ST12 ST13 ST14 ST16 to cableCR13 an dCR14
output to recorder
Sortie (vers Enregt)
CARTE INTERCONNEXION INTERCONNECTION CARD
(FACE ARRIERE) rear panel
PCM MULTIPLEXER TIMING DIAGRAMS
CHRONOGRAMMES MULTIPLEXEUR PCM
Frame
Cycle
(1 channel)
sample n
échantillonne n
converts n
converti n
samples
échantillonne (n-1)
holds
bloquetn
parity
LOGIQUE
MA1142/0
Record logic card



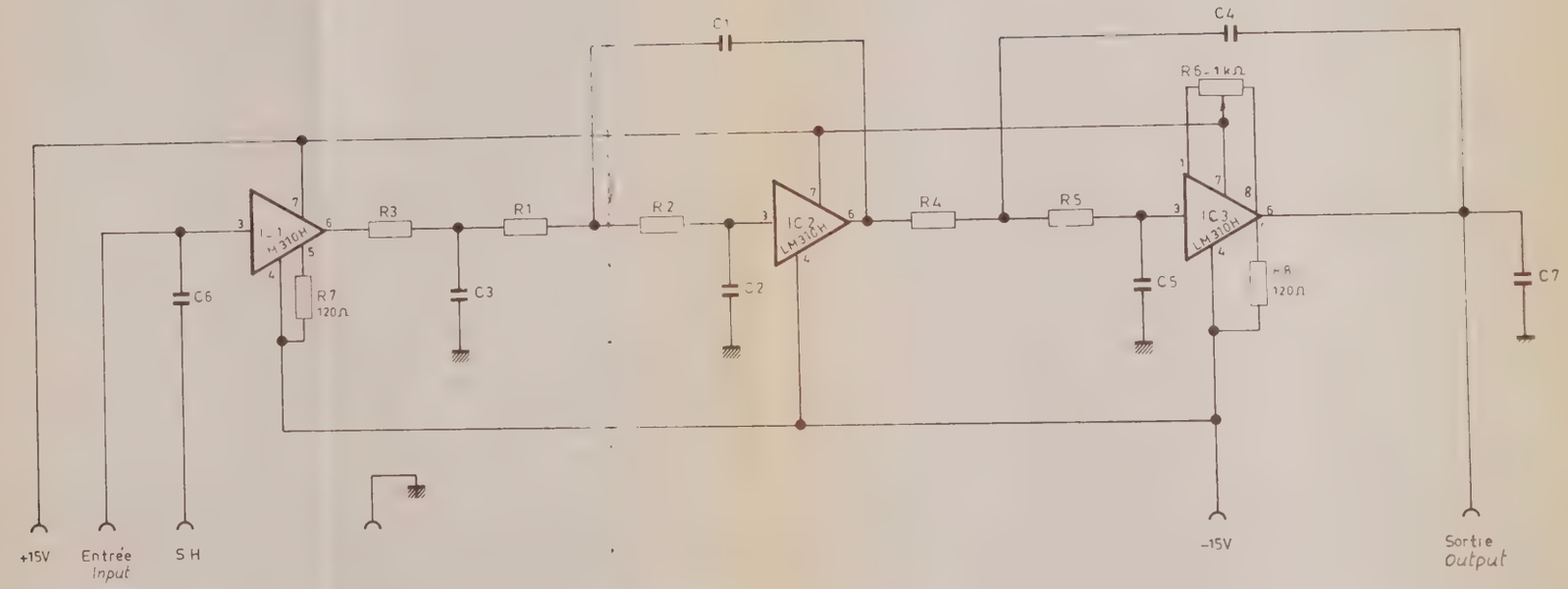
Reproduce logic card 1
CARTE LOGIQUE LECT 1



Reproduce logic card 2
CARTE LOGIQUE LECT 2



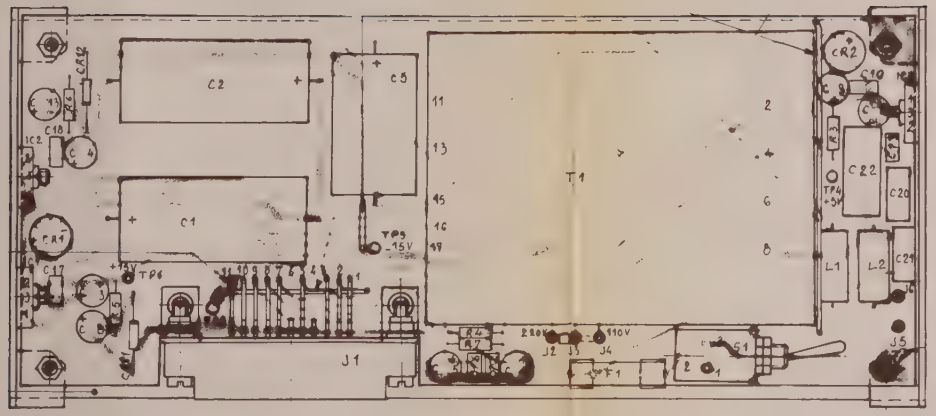
Reproduce logic card



FILTER

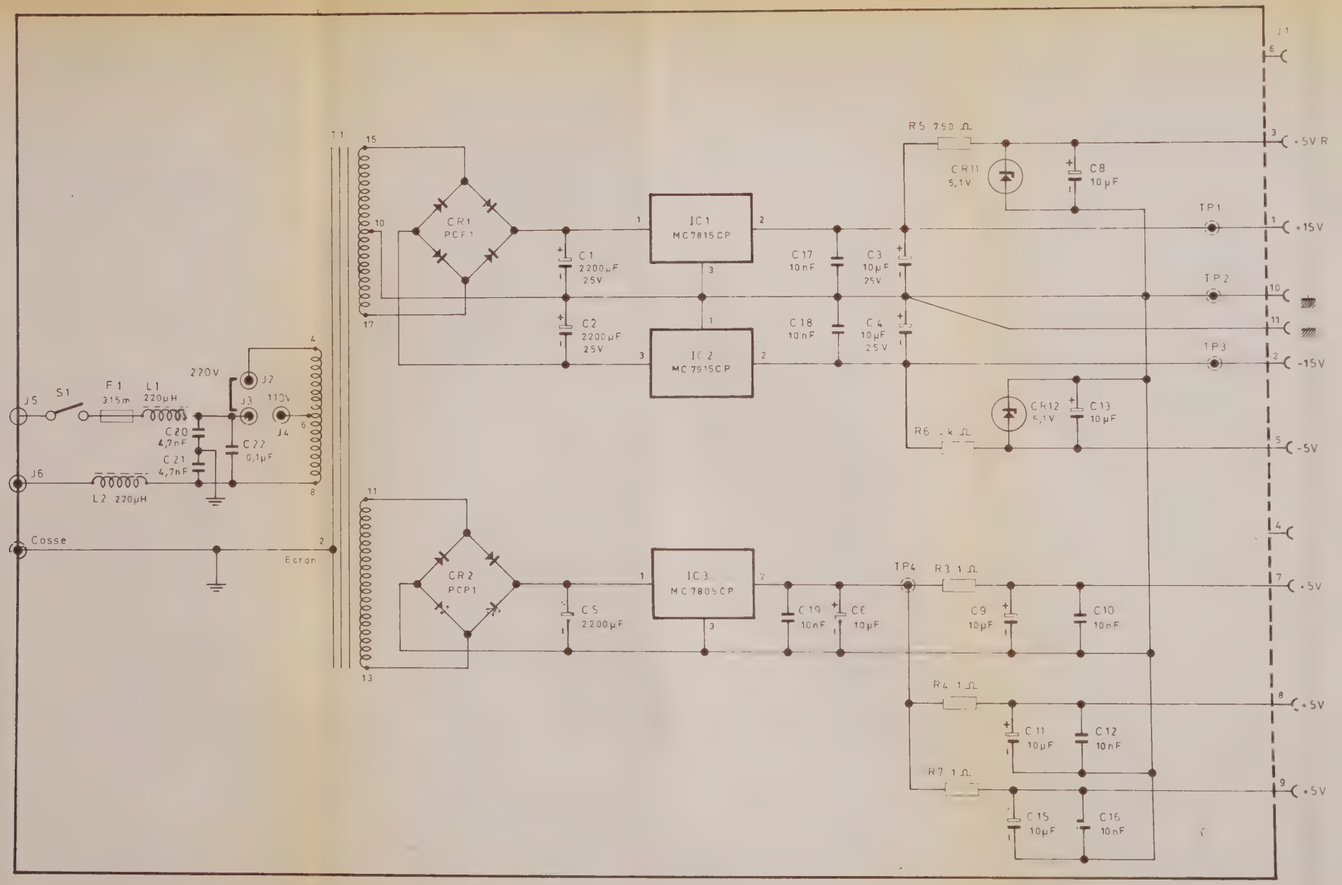
FILTRE	R1	R2	R3	R4	R5	C1	C2	C3	C4	C5	C6	C7
32 kHz	887 Ω	1650 Ω	1330 Ω	4420 Ω	732 Ω	22,5nF	1nF	10nF	33,2nF	220nF	1nF	1nF
16 kHz	1780 Ω	3320 Ω	2670 Ω	8870 Ω	1470 Ω							
8 kHz	3570 Ω	6650 Ω	5360 Ω	17400 Ω	2940 Ω							
4 kHz	7150 Ω	13,30 kΩ	10,5 kΩ	34800 Ω	5900 Ω							
2 kHz	649 Ω	1270 Ω	931 Ω	4870 Ω	845 Ω	464nF	22,5nF	226nF	464nF	3,16nF	10nF	
1 kHz	1270 Ω	2550 Ω	1870 Ω	9760 Ω	1690 Ω						10nF	
500 Hz	2550 Ω	5110 Ω	3740 Ω	19600 Ω	3400 Ω						100nF	
250 Hz	5110 Ω	10200 Ω	7500 Ω	39200 Ω	6810 Ω							
125 Hz	10,2 Ω	20,5 Ω	15 kΩ	78700 Ω	14000 Ω							
62,5 Hz	20,5kΩ	40,2kΩ	30,1 kΩ	158kΩ	26700 Ω						470nF	
31,25 Hz	41,2 kΩ	80,6kΩ	60,4kΩ	316kΩ	54900 Ω							
15,62 Hz	82,5kΩ	162kΩ	118kΩ	634kΩ	107kΩ							

16 channel PCM multiplexer filter
FILTRE MULTIPLEXEUR PCM 16 VOIES



Power supply card

CARTE ALIMENTATION



Power supply

ALIMENTATION

SP031332

2 FILTRES 1

4 FILTRES 3

6 FILTRES 5

8 FILTRES 7

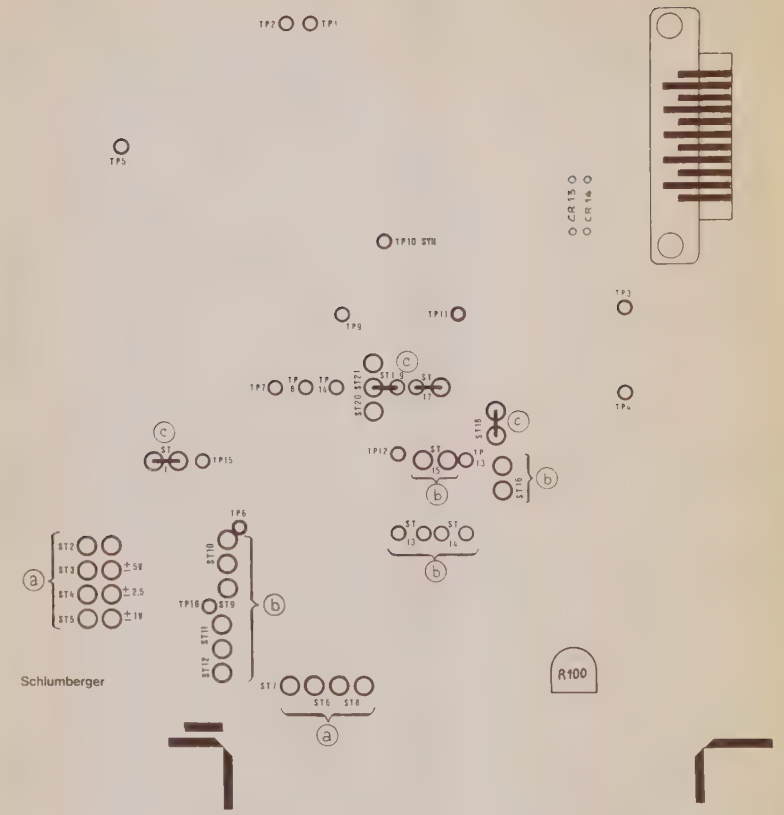
10 FILTRES 9

12 FILTRES 11

14 FILTRES 13

16 FILTRES 15

58034698



ⓐ *Choix du niveau d'entrée*

niveaux entree	straps a effectuer
± 5V	ST3 _ ST6
± 2,5V	ST2 _ ST4 _ ST6
± 1V	ST2 _ ST6 _ ST5
0 à 2V	ST2 _ ST5 _ ST8
0 à 5V	ST3 _ ST7 _ ST8

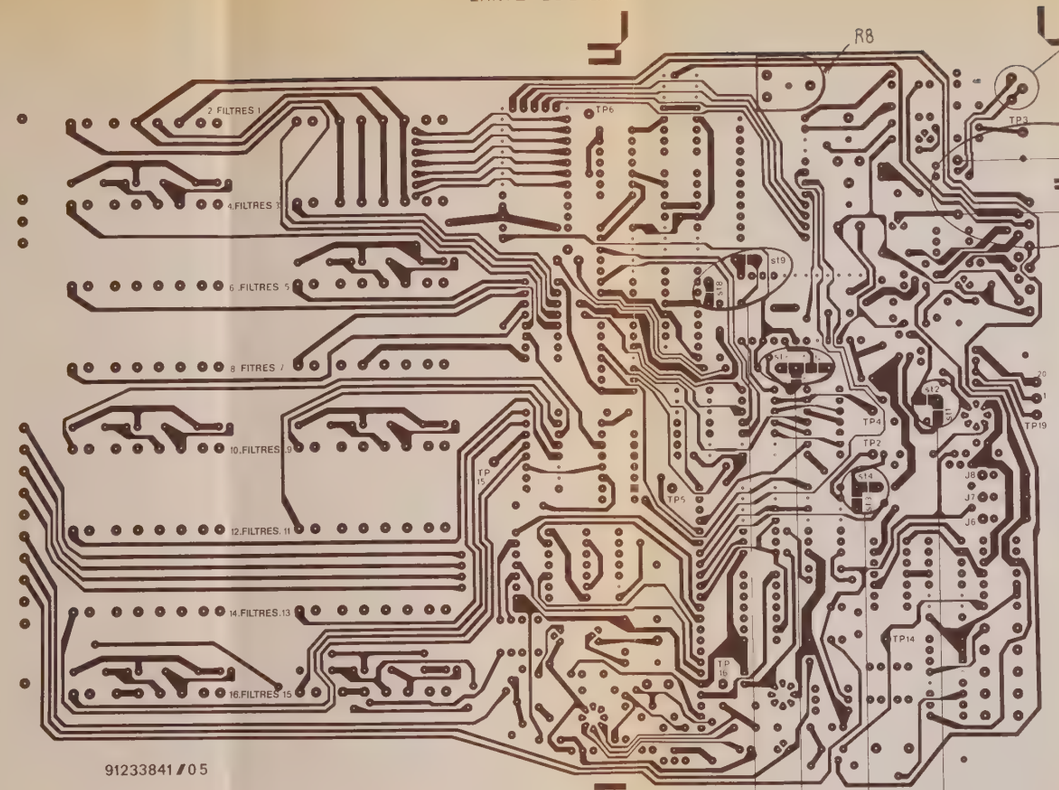
ⓑ *Version 10 ou 12 bits*

Nombre de bits	straps à réaliser
10 bits	ST9 _ ST11 _ ST15
12 bits	ST10 _ ST12 _ ST13 _ ST14 _ ST16 CR13 _ CR14

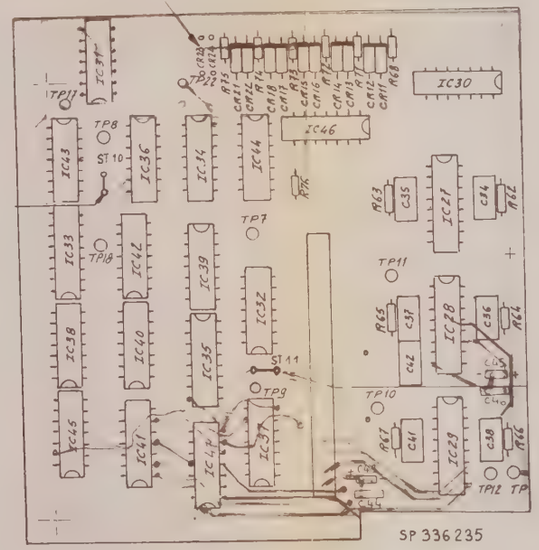
ⓒ *ne pas modifier la position de ces cavaliers*

Multiplexeur MA1142

CARTE LOGIQUE 1



CARTE LOGIQUE 2



C4 / R6 – Correction de phase	
Cadence de bits	C4
14 bits	330 pF
500 kbit	680 pF
250 kbit	1000 pF
125 kbit	2,2 nF
62,5 kbit	4,7 nF
31,25 kbit	10 nF
15,6 kbit	22 nF
7,8 kbit	47 nF

st 1, st 2 : choix du standard

Choix du standard	
LBG 2	st 1
tous les autres standards	st 2

st 3, st 4 : inversion du message

Inversion du message	
st 3	message inverse
st 4	message normal (livré câblé en st 4)

st 5, st 6, st 7, st 12 : choix de la tension de sortie

Choix de la tension de sortie	
+ 5 V	st 5
± 2,5 V	st 5 – st 6
± 1 V	st 5 – st 7
0 à 2 V	st 7 – st 12
0 à 5 V	st 6 – st 12

option 10 ou 12 bits	
st 8, st 9	câblés pour 12 bits
10 bits non câblés (livrés non câblés)	

Démultiplexeur MA 1233

CHAPTER V

MA 1142 / MA 1233

MULTIPLEXER/DEMULTIPLEXER UNIT

MAGNETIC TAPE RECORDER ADAPTATION

Issue : FEBRUARY 1979

MA 1142/MA 1233 MULTIPLEXER/DEMULTIPLEXER UNIT

MAGNETIC TAPE RECORDER ADAPTATION

The information presented in the present manual is based on the assumption that the reader is familiar with the following :

- MA 1142/MA 1233 operating manual
- adjustment procedures for the magnetic recorder concerned.

Preliminaries

Static adjustment

Before connecting the multiplexer/demultiplexer unit to the magnetic recorder, check correct operation of the former under static conditions (without using the magnetic tape).

Proceed as follows :

1) Check :

   a) that bit rates correspond to recorder bandwidth (see recorder manual)

   b) that the filters inserted in the multiplexer correspond correctly to the number of channels selected according to bit rate

   c) that in the absence of these input filters, their place is taken by input attenuators

   d) that in the absence of output filters in the demultiplexer, their place is taken by memory cards.

2) Connect output of the MA 1142/0 (record) to input of the MA 1233/0 (reproduce), via a BNC lead. The green lamp should come on.

3) Adjust the VCO control to its mid-way position. The green lamp should go out to right or left of this position.

4) Use a signal generator and oscilloscope to check :

   - correct operation of the channels
   - bandwidth or ladder steps (if memory card used)
   - input and output levels.

I - UTILIZATION WITH TYPE MT 5528 OR MT 5530 MAGNETIC RECORDERS

Type MT 5528 or MT 5530 magnetic recorders can be equipped with brass or hard pole tip magnetic heads. Brass heads are recognizable by their yellow colour, while hard pole tip heads are grey.

NOTE : Before inserting Direct mode reproduce channels, check the type of heads used on the recorder. Then proceed as indicated below :

- If the recorder is equipped with brass heads, use the following Direct mode amplifiers :
  - MA 2114/0 record cards
  - MA 2219/0 reproduce cards.
- If the recorder is equipped with hard pole tip heads, use the following Direct mode amplifiers :
  - MA 2114/0 record cards
  - MA 2219/1 reproduce cards.

In the case of MA 2219/1 reproduce cards, check that the phase and HF equalizer capacity values comply with those shown in brackets on the diagram (see attached documents).

1.1 - Checking the complete record/reproduce system for Direct mode

1) Move the Direct record amplifier input sensitivity selector to the "1 V rms" position.

2) Move the switch on the front face of the Direct reproduce amplifier to "IRIG".

3) Select the tape speed corresponding to a bandwidth compatible with the bit rate selected on the multiplexer/demultiplexer unit.

4) Inject a 1 kHz sine-wave signal of 1 V rms.

5) Load a pre-erased tape on the magnetic recorder.

6) Connect the recorder to line supply, and switch on.

7) Depress the "Forward" and "Record" pushbuttons.

8) Check the response curve (see data sheet). This should fall within a ± 3 dB band.

9) Short input, and check S/N ratio. This should be compatible with the specifications given in the data sheets.

If an incorrect result is obtained, refer to the Maintenance Manual, and carry out the adjustments described in paragraph 3.10.2.1 (page 3.68), and paragraph 3.11.4.4 (page 3.76) (see attached document).

NOTE : To ensure correct operation of the multiplexer/demultiplexer unit, Direct channels must be properly adjusted, and output level must be 1 V rms for full scale.

1.2 - Connection of MA 1142 and MA 1233

1) Using the oscilloscope, check that the level picked off the BNC output connector is close to 3 V peak. The signal displayed should be square-wave in form, with a pseudo-random repetition frequency. This voltage can be adjusted on control R100 (see Operating Manual).

2) Connect output of the MA 1142 to input of the previously checked Direct channel.

3) Connect input of the MA 1233 to reproduce output of the previously checked Direct channel.

4) Depress the "Forward" and "Record" pushbuttons.

5) Check that the green "VCO" lamp is on.

NOTE : It is normal for the "saturation" lamp on the reproduce amplifier to flicker slightly.

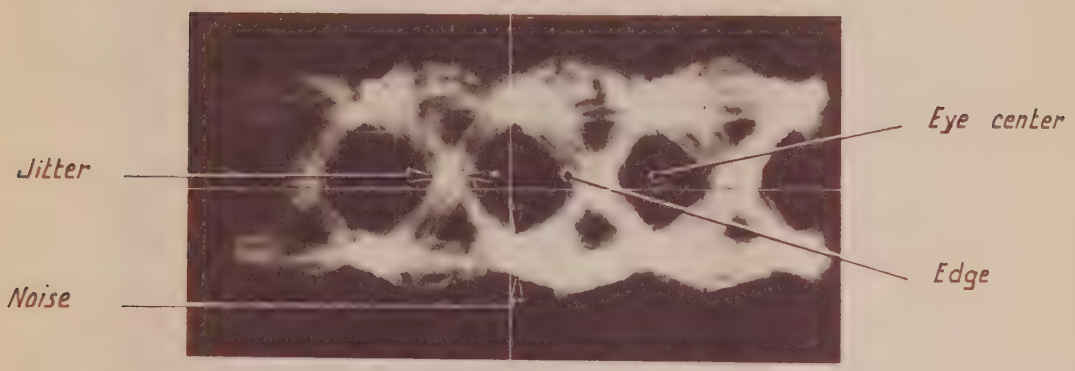
1.3 - Complementary adjustment

1) Connect an oscilloscope to the digital output connector :

a) vertical input : pin 15
b) ground : pin 16
c) external trigger : pin 22 (clock).

2) Adjust oscilloscope sweep rate so as [illegible] sections.

3) Adjust bias HF so as to obtain the [illegible] edges should be as far as [illegible].



II - UTILIZATION WITH TYPE MP [illegible]

Adjustment procedures described for the [illegible] However, the following points should be [illegible]

1) As the MP 5522 is equipped exclusively [illegible] type MA 2219/0 Direct mode reproduce amplifiers are [illegible].

2) Depress the "Record" and "Erase" push [illegible].

III - UTILIZATION WITH TYPE MP 5421 [illegible]

These recorders are equipped exclusively [illegible] Direct mode reproduce amplifiers must be [illegible].

- Refer to the adjustment procedures described [illegible] 1 and 2 concerning utilization with type [illegible].

- After adjusting the Direct channels, and before connecting the multiplexer/demultiplexer unit, carry out the following check :

3.1 - Checking response under pulse conditions

1) Record positive pulses of 1 V peak at a repetition rate of 1/10 maximum bandwidth, and with a width of 2/BW (BW = bandwidth in Hz).

2) Display the pulses appearing at reproduce output on an oscilloscope (checking that connector polarity is correct).

The positive pulses recorded should be reproduced also in positive form. If this is not the case, make one or other of the following modifications :

- Reverse record head wiring
- Reverse data direction in the demultiplexer.

Proceed as follows :

a) Open the MA 1233 (see manual).
b) Unsolder strap ST4 (see attached figure).
c) Solder strap ST3 (see attached figure).

IV - UTILIZATION WITH TYPE ML 2601 MAGNETIC RECORDER

Run a direct check (not using the magnetic tape) on correct operation of the multiplexer/demultiplexer unit (see "preliminaries", page 1).

- Check that Direct record mode and IRIG Intermediate band (IB) standard have been selected on the ML 2601.

- Set the Direct record amplifier for an input level of 1 V rms (see manual page 2.9, paragraph 2.1.7.1.1).

- Check reproduce output level at a frequency of 1 kHz. A value of 1 V rms should be obtained. If this is not the case, adjust level on the Gain control on the front face of the MA 2228/0 reproduce amplifier.

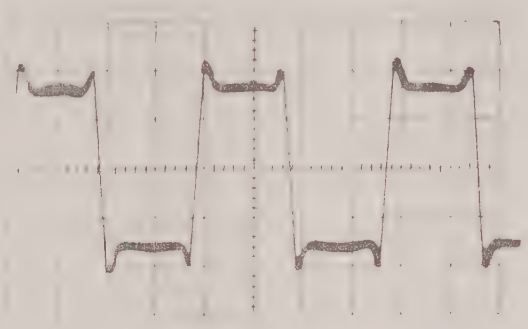
- Select tape speed according to the bandwidth corresponding to selected bit rate.

- Check the response curve of the complete record/reproduce system at selected tape speed. The curve should fall within a $\pm$ 3 dB band (see data sheet).

- Short record amplifier input, and check S/N ratio. This should comply with the specifications indicated in the data sheets.

- Inject a square-wave signal with an amplitude of 2.8 V peak, and a frequency of 1/10 bandwidth for the Direct channel (BP/10), at record input.

- Display the signal picked off reproduce output on an oscilloscope. A form identical to that shown in the figure below should be obtained.



If the response curve of square-wave signal response is incorrect, readjust the Direct channels, following the instructions given in the Maintenance Manual (page 3.80, paragraph 3.28.2 for Direct record amplifiers, and page 3.87, paragraph 3.29.2 for Direct reproduce amplifiers : see attached document).

4.1 - Connecting the MA 1142 and MA 1233

1) Use the oscilloscope to check that the level appearing on the BNC output connector of the MA 1142 is approx. 3 V rms. The signal displayed on the oscilloscope should be square-wave, with a pseudo-random repetition frequency. This voltage can be adjusted on control R100 (see Operating Manual).

2) Connect output of the MA 1142 to input of the Direct channel previously checked.

3) Connect input of the MA 1233 to reproduce output of the Direct channel previously checked.

4) Depress the "Forward" and "Record" pushbuttons.

5) Check that the green "VCO" lamp is on.

4.2 - Operation of multiplexer/demultiplexer unit on WBG2 standard

The ML 2601 can be equipped for WBG2 operation, plus extending autonomy (according to bandwidth and number of channels multiplexed).

- Use the Direct channel adjustment procedure as indicated above, allowing for the different characteristics of the magnetic recorder.

Note : Before connecting the multiplexer/demultiplexer unit, a strap must be changed on the MA 1233.

Proceed as follows :

1) Open the MA 1233 (see manual).

2) Unsolder strap ST2 (see figure attached).

3) Solder strap ST1 (see figure attached).

4) Connect the multiplexer/demultiplexer unit to the recorder (see paragraph A).

5) If the green "VCO" lamp does not come on, or flickers, readjust control R8 as necessary.

6) Close the MA 1233.

NOTE : The MA 1233 can be factory-preset for WBG2 operation, if specified in the purchase order.

CHAPTER VI

ADAPTATION OF OTHER MAGNETIC RECORDERS TO THE MA 1142/MA 1233 MULTIPLEXER/DEMULTIPLEXER UNIT

Preliminaries

Before connecting the multiplexer/demultiplexer unit to the magnetic recorder, check correct operation of the former under static conditions (without using the magnetic tape).

Proceed as follows :

1) Check :

a) that bit rates correspond to recorder bandwidth (see recorder manual)

b) that the filters inserted in the multiplexer correspond correctly to the number of channels selected according to bit rate

c) that in the absence of these input filters, their place is taken by input attenuators

d) that in the absence of output filters in the demultiplexer, their place is taken by memory cards.

2) Connect output of the MA 1142/0 (record) to input of the MA 1233/0 (reproduce), via a BNC lead. The green light should come on.

3) Adjust the VCO control to its mid-way position. The green lamp should go out to right or left of this position.

4) Use a signal generator and oscilloscope to check :

- correct operation of the channels
- bandwidth or ladder steps (if memory card used)
- input and output levels.

I - IRIG STANDARD RECORDERS

The multiplexer/demultiplexer unit is designed for operation with Direct channels. These channels must be correctly adjusted and phase-compensated.

Carry out the following checks :

1) Check that the recorder is prepared for IB standard operation.

2) Select a tape speed corresponding to the bit rate to be recorded.

3) Adjust input and output levels to obtain 1 V rms at reference frequency.

4) Check bandwidth. It should fall within a $\pm$ 3 dB band (see recorder manual).

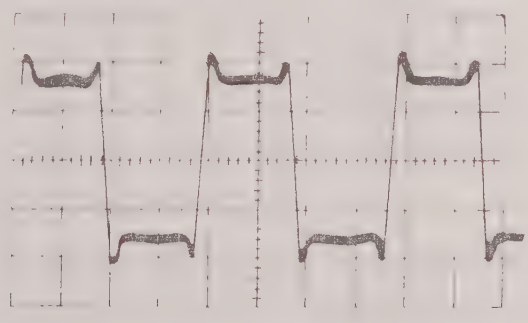
5) Check S/N ratio, which should be > 20 dB.

6) Check recorder phase response, proceeding as follows :

   a) Record square-wave signals at a repetition frequency corresponding to 1/10 of bandwidth.

   b) Display the reproduce signals on an oscilloscope.

These signals should have a form identical to that shown in the figure below.

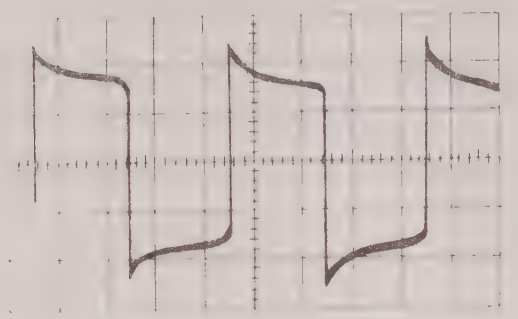


   c) Record positive pulses at a repetition frequency corresponding to 1/10 of bandwidth, and a width of 2/bandwidth.

   The positive pulses recorded should be reproduced also in positive form.

In the event of phase response anomalies, readjust phase equalization on the recorder. Certain machines do not have phase equalization.

In this case, the form of the square-wave signals is as shown in the figure below :



Adjust phase equalization inside the demultiplexer (see Operating Manual paragraph 2.2.2.1), after recording the multiplexer/demultiplexer unit to the recorder.

If pulse response anomalies are observed, make one or other of the following modifications :

- Reverse record head wiring
- Reverse data direction in the demultiplexer.

Proceed as follows :

a) Open the MA 1233 (see manual).
b) Unsolder strap ST4 (see figure attached).
c) Solder strap ST3 (see figure attached).

NOTE : For all the above operations, use a pre-erased magnetic tape.

1.1 - Connecting the MA 1142 and MA 1233

1) Use the oscilloscope to check that the level appearing on the BNC output connector of the MA 1142 is approx. 3 V rms. The signal displayed on the oscilloscope should be square-wave, with a pseudo-random repetition frequency. This voltage can be adjusted on control R100 (see Operating Manual).

2) Connect output of the MA 1142 to input of the Direct channel previously checked.

3) Connect input of the MA 1233 to reproduce output of the Direct channel previously checked.

4) Select the record function.

5) Check that the VCO lamp is on.

I.2 - Operation of the multiplexer/demultiplexer unit on IRIG standard WBG2

The multiplexer/demultiplexer unit is also designed for operation on WBG2. If this standard is used, follow the check procedures described above, allowing for the different characteristics of the magnetic recorder.

Before connecting the multiplexer/demultiplexer unit, a strap must be changed in the MA 1233 demultiplexer.

Proceed as follows :

- Open the MA 1233 (see manual).
- Unsolder strap ST2 (see figure attached).
- Solder strap ST1 (see figure attached).
- Connect the multiplexer/demultiplexer unit to the recorder (see § I.1).
- If the green "VCO" lamp does not come on, or flashes, readjust control R8.
- Close the MA 1233.

NOTE : The MA 1233 can be factory-preset for WBG2 operation, if specified in the purchase order.

II - AUDIO TYPE MAGNETIC RECORDERS

These recorders have a response curve between 20 Hz and 20 kHz, according to model and tape speed.

- they do not have phase equalization
- they show approx. 10 dB pre-emphasis for record.

Before connecting the recorder to the multiplexer/demultiplexer unit, carry out the checks defined for IRIG standard recorders, taking the following additional precautions :

a) Adjust input level to 1 V rms at 1 kHz, sub-modulating by 10 dB with respect to peak output level.

b) Adjust output level to 1 V rms.

c) Check bandwidth.

d) Note limit points of bandwidth. These should fall within a tolerance of $\pm$ 3 dB.

e) Select the bit rate corresponding to the bandwidth value observed at step d) above.

f) Connect the multiplexer/demultiplexer unit, following the instructions given in § 1.1.

CHAPTER VII

MT 5528 MAINTENANCE MANUAL (EXTRACT)

3.10.2 - Adjustment of Direct record amplifiers

Equipment required

- Generator
- Oscilloscope
- Digital voltmeter
- AC voltmeter (PHILIPS PM 2454 or equivalent).

3.10.2.1 - Adjustment of HF bias

- Run the tape transport in the RECORD mode at tape speed :

  MT 5530, ML 1530 and MT 5528 : 152 cm/s
  MP 5521/2 and MP 5522 : 76 cm/s
  MP 5521/3 and MP 5421 : 34 cm/s.

Plug the following cards into the channel to be adjusted :

- MA 2114/0 record amplifier
- MA 2219/0 reproduce amplifier (of MA 2219/1 in the case of hard pole tip heads).

Apply a voltage at input, with frequency as follows :

MT 5530; ML 1530 and MT 5528 : 250 kHz
MP 5521/2 and MP 5522 : 125 kHz
MP 5521/3 and MP 5421 : 62.5 kHz

with level according to selected measurement range (rms).

- Connect an AC millivoltmeter to reproduce output of the channel concerned.

- Adjust HF control R41 on the front face of the record amplifier, to obtain maximum reproduce level. When this value is reached, turn the HF control clockwise until the voltmeter pointer gives a reading 3 dB below the maximum value previously obtained.

- HF bias is now adjusted in accordance with IRIG standards.

NOTE : No readjustment is required when tape speed is changed.

3.10.2.2 - Checking the SATURATION lamp

Use a generator to inject a sine-wave signal of 1 V rms at 1 kHz, and check that the voltage readings on the test points comply with the values indicated on the general diagram.

Increase input signal level progressively. The "SATURATION" lamp should come on for a voltage of 1.2 V.

3.10.2.3 - Checking HF bias current

- Disconnect the generator.
- Connect a voltmeter between TP 3 and TP 2.
- Depress the "Record" pushbutton.
- Operate core T1 to check that voltage value is maximum, tuned on 1.5 MHz.
- Check that the adjustment range of front face control R41 corresponds to HF bias current variation between 30 and 250 mV rms ± 15 %.
- Connect the oscilloscope to the collector of Q2, and adjust the core of L5 so as to obtain minimum residual HF voltage.

3.10.2.4 - Checking the ALARM lamp

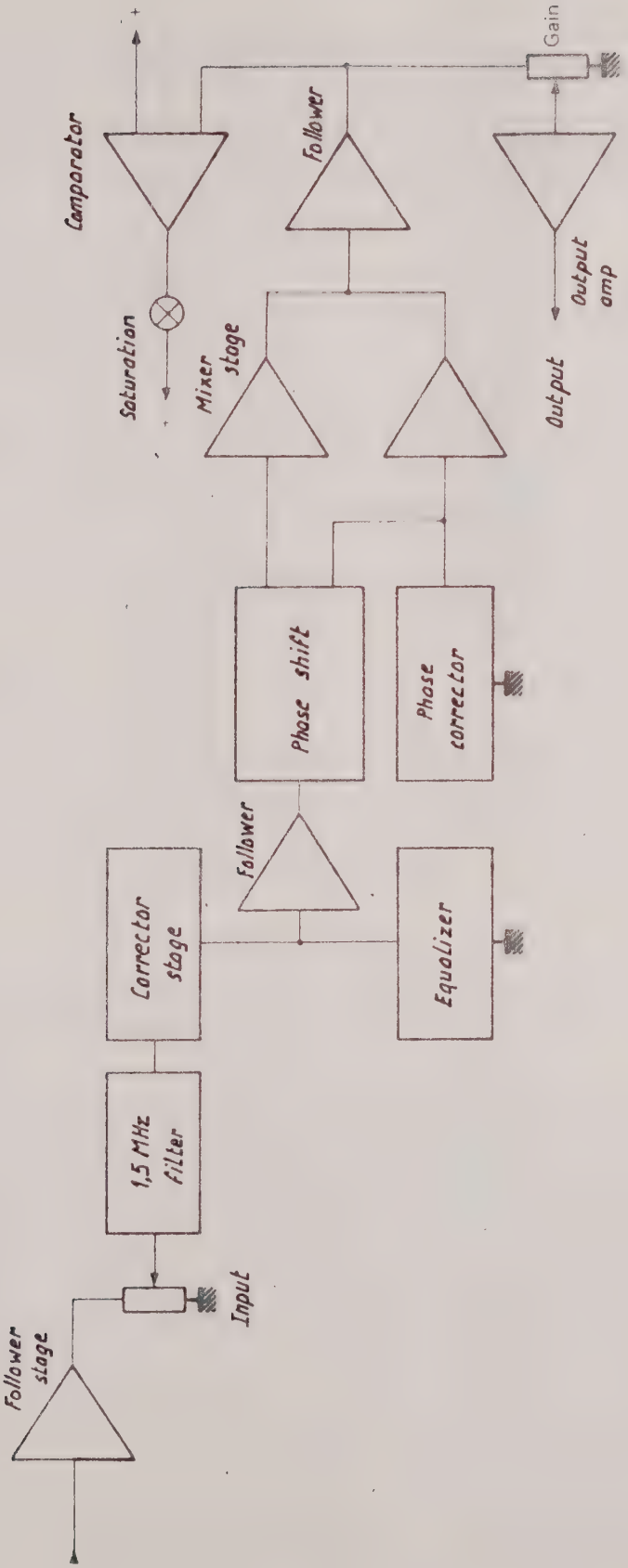
This lamp should come on :

1) for an HF bias current below 90 mV rms ± 15 %
2) if the jumper between J2 and J3 is removed. Remember to replace the jumper.

3.10.2.5 - Adjustment of LF gain (HF disconnected)

This adjustment is made in the factory. Readjustment is only required following replacement of components.

- If necessary, adjust R14 to obtain 18 mV rms between TP3 and ground (TP2), injecting a 1 V rms signal at 1 kHz at input of the channel to be adjusted.


Follower stage
Input
1,5 MHz filter
Corrector stage
Equalizer
Follower
Phase shift
Phase corrector
Mixer stage
Saturation
Comparator
Follower
Gain
Output amp
Output

3.11 - MA 2219/0 (Plate 14) or MA 2219/1 Direct reproduce amplifier

Reproduce is practically simultaneous with record, and the signal is available at output as soon as the recorded section of tape passes across the reproduce head.

The "SATURATION" lamp on the front face comes on to indicate defective operation of the reproduce circuit.

A selector on the front face of the card gives a choice of two positions :
"500 Hz" : linear frequency response from 500 Hz to upper limit.
"IRIG" : linear frequency response over IRIG bandwidth.

This amplifier has automatic equalizer switching according to tape speed.

3.11.1 - Operation

The signal from the reproduce head (approx. 100 µV rms at 1 kHz), is preamplified and sent to the Direct reproduce card, on a follower stage comprising emitter follower Q1. Sensitivity threshold is adjusted on control R4. This control should be set at maximum value.

Filter L1-C3-C4 is used to eliminate perturbation resulting from the bias HF, when the recorder is operating in the simultaneous RECORD/REPRODUCE mode. D4 is used to adjust HF level minimum.

Output from the filter and follower stage drives a corrector stage, transistor Q3 giving constant amplitude/frequency reproduction. Transistor Q3 operates at constant current, regulated by transistor Q2 which corrects any variations appearing on the face of Q3.

The equalizer circuits are switched to the terminals of transistor Q3, according to tape speed :

Speed	Switching transistor
4.75 cm/s	Q47
9.5 cm/s	Q46
19 cm/s	Q45
38 cm/s	Q44
76 cm/s	Q43
152 cm/S	Q42

These equalizers give constant voltage irrespective of frequency (and therefore of tape speed). Q3 drives transistor Q4 direct.

This constant voltage is picked off the terminals of transistor Q4, used in the emitter-follower mode, and applied to the base of transistor Q5, used as a phase-shift.

The signals appearing on the terminals of the emitter and collector of Q5, drive transistors Q6 and Q7, used as mixers.

Phase correction is applied to the base of transistor Q6 :

Speed	Phase correction control transistor
4.75 cm/s	Q54
9.5 cm/s	Q53
19 cm/s	Q52
38 cm/s	Q51
76 cm/s	Q48

The signal obtained on the collectors of Q6 and Q7 is thus frequency and phase equalized.

The phase linearity obtained makes it possible to transmit square wave signals or pulses, with approx. 20 % overshoot in accordance with IRIG recommendations, without affecting signal rise time or the amplitude response curve in the selected band.

The phase equalization function is switched automatically by the tape transport speed selector.

Mixer stage Q6-Q7 drives a follower stage, comprising transistor Q8.

GAIN control R33 is inserted at output.

Control R33 is followed by the "500 Hz/IRIG" selector.

In the "500 Hz" position, the signal transits via C18. Noise dynamic range is improved, but bandwidth is slightly reduced (500 Hz).

In the "IRIG" position, C21 is placed in parallel with C18, extending the bandwidth up to 100 Hz.

The signal then reaches transistor Q12, used in the follower mode (this is the summing point for the reproduce signal and negative feedback from push-pull Q15-Q16).

The signal from Q12 via C23-R42, is amplified by transistor Q13, preceeding follower transistor Q14.

Diodes CR2-CR3 are used to avoid transistors Q15 and Q16 conducting to each other, and to set the base-emitter voltage of these same transistors.

Transistors Q15 and Q16 are used in the complementary push-pull mode, and deliver a low impedance signal.

3.11.2 - "SATURATION" lamp

The Direct reproduce amplifier has a "SATURATION" lamp.

The signal picked off the emitter of W8 is applied, via C29, to non-inverting input (2) of integrated circuit IC1.

Inverting input (3) is set at a positive voltage, adjustable on control R61.

When the voltage from Q8 goes over the threshold voltage, output of IC1 becomes positive, saturating Q17 and driving the "SATURATION" lamp.

Control R61 is set at more than 3 dB over the GAIN adjustment level.

3.11.3 - Speed switching

Speed codes A - B - C are applied to binary decoder IC2.

IC2 output	2	3	4	5	6	7
Speed (cm/s)	4.75	9.5	19	38	76	152

Each output is followed by a transistor (Q62 to Q67), controlling switching of the capacitors limiting bandwidth towards the higher frequencies by transistors Q55 to Q58 and Q61, the phase equalizer capacitors by transistors Q48 and Q51 to Q54, and the equalizers by transistors Q48 to Q47.

Bandwidth limitation towards the lower frequencies is set at 300 Hz for 152 cm/s by R82, switched by Q41, 200 Hz for 76 cm/s by R81, switched by Q38, and 100 Hz for the other, lower tape speeds, by R78.

3.11.4 - Adjustment of Direct reproduce amplifiers

Equipment used

- Oscilloscope
- Generator
- AC voltmeter (graduated in dB)
- Analyser

An accurate test rig is required for debugging this card.

Test procedure (Maintenance Department) is as follows :

3.11.4.1 - Adjustment of distortion rate

Factory adjustment

Inject a 6 kHz frequency. Measure third order harmonic level with an analyser. A reading of 1 % should be obtained. If this is not the case, adjust R14.

- Record a 1 kHz sine-wave signal at all tape speeds, and on each tape track.
- Reproduce this signal, checking that bandwidth values comply with IRIG requirements (0 to 75 kHz) at ± 3 dB.

Bandwidth at ± 3 dB (kHz)	0.1 to 9	0.1 to 18	0.1 to 37	0.1 to 75
Reference (kHz)	0.75	1.5	3	6

3.11.4.2 - GAIN adjustment

Conditions : Card mounted on test adaptor
Tape transport stopped.

a) Connect a voltmeter between TP4 (data output) and TP3 (ground).

b) Move the front face selector to "IRIG".

c) Inject a 1 kHz sine-wave signal with a level of approx. 8 mV rms at input.

d) Input control R4 should be in its maximum position. Adjust if this is not the case.

e) Adjust R33 to obtain 1 V rms ± 10 mV at output (in the case of saturation, readjust R4).

3.11.4.3 - Adjustment of output amplifier

Conditions : Card mounted on test adaptor
Tape transport stopped.

a) Connect a digital voltmeter between ground (low) and the common point of R54-R55-C52 (+).

Switch the recorder on.

Allow a few minutes for stabilization. Read off the digital voltmeter, and adjust control R44 to obtain :

0 V ± 30 mV.

b) Connect a voltmeter to the terminals of R53 (200Ω).

A DC voltage between 400 and 800 mV should be obtained on the terminals of R53 (corresponding to a quiescent current of 2 to 4 mA).

If this is not the case, readjust R48.

3.11.4.4 - Adjustment of 4.75 cm/s equalizer (selector on "IRIG")

CAUTION : The bias current must be adjusted on the record amplifiers (see § 3.10.2.1) before hand.

Conditions : Tape running at 4.75 cm/s RECORD mode (clean tape).

a) Inject a 100 Hz sine-wave signal of 1 V rms at input of the record amplifier. Move control R4 to its maximum position (fully clockwise). If not yet done, adjust R33 to obtain a level of 1 V rms at output.

b) Inject a 0.937 kHz signal of 1 V rms, and adjust R113 to obtain 1 V rms at output. ⋆

c) Inject a 9.375 kHz signal of 1 V rms, and adjust R112 to obtain 1 V rms at output. ⋆

⋆ If impossible, readjust R33.

d) Recheck b) and c) alternately, to take account of inter-action between these adjustments.

3.11.4.5 - Adjustment of equalizers for 9.5 to 152 cm/s

Input : 1 V rms Output : 1 V rms ± 3 dB

Speed (cm/s)	Data 1		Data 2		Data 3		Data 4	
	F 1 Hz	Adjust	F 2 Hz	Adjust	F 3 Hz	Adjust	F 4 Hz	Adjust
9.5	100	none	1562.5	R 107	15625	R 106	9375	none
19	100	"	3125	R 103	31250	R 102	18750	"
38	100	"	6250	R 97	62500	R 96	37500	"
76	200	"	12500	R 93	125000	R 92	75000	"
152	300	"	25000*	R 87	250000	R 86	150000	"

* Check that the 3 dB tolerance is observed at 30 kHz, 300 kHz, and sub-multiples.

Note : - 1 - Data 4 : Adjust the self-inductor core if necessary.
- 2 - Adjust with screen fixed to card.

ML 2601 MAINTENANCE MANUAL (EXTRACT)

3.28.2 - Adjustment of MA 2130/0 Direct record amplifier (Plate 11)

Equipment required :

- Oscilloscope
- Current measurement probe
- Generator
- RMS millivoltmeter
- Lead (jack/BNC)
- Screwdriver.

See fig. 3-15.

3.28.2.1 - Adjustment of LF stages

Note : Check record/reproduce head standard (WBG1 or WBG2).

1 - Switch the recorder off.

2 - Extract the MA 2130/0 amplifier from its nest.

3 - Remove the shield on the MA 2130/0, undoing the two countersunk shield attachment screws.

4 - Place the MA 2130/0 on a test adaptor.

5 - Disconnect "HF output" BNC connector J310 (rear face of control module).

6 - Move selector S1 (input impedance) to "20 kΩ".

7 - Move selector S2 (input sensitivity) to "1 - 10 V rms".

8 - Move selector S3 to "WBG1" (3.5 MHz) or "WBG2" (7 MHz).

9 - Select standard 3 or 4 (front panel of control module).

10 - Move front face GAIN control R7 to its maximum position (fully clockwise).

11 - Connect the millivoltmeter and oscilloscope to "display output" (TP1).

12 - Switch the recorder on. ("ϟ").

13 - Select tape speed 152 cm/s.

14 - Inject a 1 V rms sine wave signal at 1 kHz (IB) or 10 kHz (WBG2) at record input.

15 - The voltage on TP1 is 0.7 V rms (2 V peak).

16 - Check that the same voltage (0.7 V rms) is obtained if 100 mV rms is injected, and moving selector S2 to the "0.1 - 1 V rms" position.

17 - Move selector S2 to "1 - 10 V rms".

18 - Disconnect the RMS millivoltmeter and oscilloscope.

19 - Connect the oscilloscope with its current measurement probe, to pin 22 (to record head).

20 - As a guide, LF record current is 14 mA for WBG1 and 6 mA for WBG2 (with the card in a fully operational state).

21 - Switch the recorder off.

22 - Disconnect the oscilloscope and the current measurement probe.

23 - Connect "HF output" BNC connector J310.

3.28.2.2 - Adjustment of HF stages

24 - Short record input.

25 - Move selector S3 to WBG1.

26 - Select standard 3 on the control module.

27 - Move front panel "HF adjust." control R39 to its maximum position (fully clockwise).

28 - Connect the RMS millivoltmeter to test point T4 on the MA 2130/0.

29 - Switch the recorder on ("ϟ").

30 - Select tape speed 152 cm/s.

31 - Depress Record pushbutton "REC".

32 - Set variable capacitor C13 to obtain minimum level on T94.

33 - Move selector S3 to "WBG2".

34 - Select standard 4 on the control module.

35 - Set variable capacitor C12 to obtain minimum level on TP4.

36 - Disconnect the RMS millivoltmeter.

37 - Remove the short on record input.

38 - Connect the oscilloscope with its current measurement probe to pin 22 (to record head).

39 - Slightly change the position of "HF adjust." control R39, to check the presence of the HF signal.

As a guide, the current value is 200 mA for WBG1, and 80 mA for WBG2 (with the card in a fully operational state).

40 - Inject a 1 V rms sine wave signal at 1 kHz (IB) or 10 kHz (WBG2) at record input (BNC connector).

41 - Check HF/LF superimposition for WBG1 or WBG2, and the action of record head current adjustment controls R21 and R22.

NOTE : Control R21 or R22 is cut in automatically by "IB/WBG2" selector S3 on the MA 2130/0.

42 - Switch the recorder off.

43 - Return the recorder to its initial state.

3.29 - MA 2228/0 direct reproduce amplifier (Plate 12).

3.29.1 - Operation

This amplifier incorporates :

- input stage,
- detachable amplitude equalizer and phase corrector circuits,
- switchable gain intermediate stage, associated with active HP filter,
- output amplifier,
- display amplifier.

3.29.1.1 - Input stage

The input stage comprises pseudo-differential amplifier Q1 to Q4, in which the load is part of the amplitude equalizer. Two switchable serial rejector circuits (L1 - T4 and L2 - T5) are used to filter out residual 7 or 3.5 MHz via HF.

3.29.1.2 - Equalizer circuit

The equalizer circuit, switched according to tape speed, has a frequency response which is the inverse of that of the record and reproduce heads. The operating principle for this circuit is based on the combination of 5 transfer functions, of the integrator/differentiator/tuned circuit type. The integrator part comprises C1 - R7, used to limit gain at low frequencies.

R6 is used for fine integration control. This adjustment is set at 1/10 of max. frequency.

The differentiator part comprises C3, R13, R12, R11 and C2. The differentiator part is adjusted (R13) to half max. frequency.

The tuned circuit comprises L1 and C2. Tuning frequency is approx. F max. + 10 %. This circuit is designed to match high frequencies, gain being adjusted to max. frequency on control R8.

Two integration operations are made on five F max. values, using C4 and C5, to limit noise at high frequencies. The phase correct circuit comprising Q8, Q11, Q12, C6, C7, R21, R23 and R14 has constant amplitude, and phase-shift varying with frequency. This circuit is used to correct phase-shift. Adjustment (R14) is made so as to obtain correct restoration of a square-wave signal, the frequency of which is 1/20 F max., or 10 times F min.

The amplifier will take eight WBG2 or IB equalizers, covering reproduce of tapes recorded at 2.38 to 304 cm/s.

3.29.1.3 - High-pass filter

The 100 Hz or 400 Hz high pass filter comprises Q13, C12, C13, R28, R31, R32 and R33. It is used to reduce noise at low frequencies.

The switchable gain intermediate stage comprises Q14, Q16, R41, R37 and R38. This stage is used for WBG2 or IB level matching.

3.29.1.4 - Output amplifier

The output amplifier uses discrete components Q18, Q21, Q22, Q23 and Q24. It has negative feedback to give a bandwidth of 2 MHz with low distortion. Output impedance is 50Ω. A 50Ω load is required to match the amplifier.

Output level can be adjusted on R26.

3.29.1.5 - Display amplifier

The display amplifier comprises Q25, R67 and R71. Control R67 is used to adjust output level ± 1 V peak.

The input and equalizer stages require particularly well-filtered power supplies. This condition is achieved by the use of power supply filter cells Q15, R42, R43, R44, C15, C16, C17 and Q17, R46, R47, R48, C21, C22, C23.

3.29.2 - Adjustment of MA 2228/O direct reproduce amplifier (Plate 12)

Equipment required :

- Oscilloscope
- Sine wave and square wave generator
- Frequency analyser
- Two RMS millivoltmeters
- 50Ω load
- Lead (jack/BNC)
- Two test adaptors
- Screwdriver

See fig. 3.16.

3.29.2.1 - Gain adjustment (IB)

1 - Switch the recorder off.

2 - Extract the MA 2228/O reproduce amplifier from its nest.

3 - Remove the shield, undoing the two countersunk shield attachment screws.

4 - Move selectors S1 to S6 to "IB".

5 - Check that the equalizers correspond to IB standard.

6 - Select standard 3 on the control module.

7 - Mount the MA 2228/O amplifier on a test adaptor.

8 - Connect the signal generator to record input (BNC connector).

9 - Connect the oscilloscope and RMS millivoltmeter to reproduce output (BNC connector).

10 - Switch the recorder on ("ϟ").

11 - Select tape speed 152 cm/s.

12 - Depress the " " and "REC" pushbuttons.

13 - Inject a 1 V rms sine wave signal of 1 kHz at record input.

14 - Check that the voltage on "display output" TP1 on the MA 2130/0 is 0.7 V rms (2 V peak). If this is not the case, readjust GAIN control R7 on the MA 2130/0 front panel.

15 - Adjust GAIN control R26 on the front panel of the MA 2228/0, to obtain 1 V rms on reproduce output.

16 - Switch the recorder off.

17 - Disconnect the oscilloscope and RMS millivoltmeter.

3.29.2.2 - Adjustment of "display output" level (IB)

18 - Connect the oscilloscope and RMS millivoltmeter to "display output" pin 5 on the MA 2228/0.

19 - Switch the recorder on (" ϟ ").

20 - Select tape speed 152 cm/s.

21 - Depress the " " and "REC" pushbuttons.

22 - Inject a 1 V rms sine wave signal at 1 kHz on record input.

23 - Adjust control R67 on the MA 2228/0, to obtain 0.7 V rms (2 V peak) on "display output" pin 5.

NOTE : This operation can be carried out on the MA 8029/0 display module.

24 - Switch the recorder off.

3.29.2.3 - Gain adjustment (WBG2)

Proceed as for IB gain adjustment, executing the following steps :

1 - 2 - 3
4 - Selectors S1 to S6 on "WBG2".
5 - Check that equalizers correspond to standard WBG2.
6 - Select standard 4 on the control module.
7 - 8 - 9 - 10 - 11 - 12
13 - Inject 1 V rms at 10 kHz on record input.
14 - 15 - 16 - 17

3.29.2.4 - Adjustment of "display output" level (WBG2)

Proceed as for IB "display output" level adjustment, executing the following steps :

18 - 19 - 20 - 21

22 - Inject 1 V rms at 10 kHz.

23 - NOTE - 24

3.29.2.5 - Adjustment of HF rejector circuits (L1 - C4 and L2 - C5)

1 - Switch the recorder off.

2 - Move selectors S1 to S6 to "IB" or "WBG2".

3 - Check that the equalizers correspond to standard IB or WBG2.

4 - Select standard 3 or 4 on the control module.

5 - Connect the RMS millivoltmeter to TP2 on the MA 2228/0.

6 - Switch the recorder on (" ϟ ").

7 - Select tape speed 152 cm/s.

8 - Depress the "REC" pushbutton.

9 - Adjust variable capacitor C5 (IB) or C4 (WBG2), to obtain a minimum voltage value on TP2.

10 - Switch the recorder off.

3.29.2.6 - Adjustment of bandwidth and S/N ratio for WBG1 or WBG2

WBG1 (IB)

1 - Switch the recorder off.

2 - Extract the MA 2130/0 record amplifier and MA 2228/0 reproduce amplifier from their nests.

3 - Remove the shield from each amplifier, undoing the two countersunk shield attachement screws.

4 - Select standard and corresponding equalizers for WBG1, and check that the record and reproduce heads are of the right standard.

5 - Mount the MA 2130/0 and MA 2228/0 amplifiers on test adaptors.

6 - Connect the generator and RMS millivoltmeter to record input (BNC connector).

7 - Connect the oscilloscope, RMS millivoltmeter and frequency analyser to reproduce output (BNC connector).

Note : Remember to load into 50Ω.

8 - Switch the recorder on (" ").

9 - Select tape speed 152 cm/s.

10 - Depress the " " and "REC" pushbuttons.

Note : Adjust HF peak if necessary (see § 1.4.4.2 and 1.4.4.3).

11 - Inject a 1 V rms sine wave signal at 1 kHz on record input.

12 - Adjust front panel GAIN control R26 on the MA 2228/0, to obtain 1 V rms on reproduce output.

13 - Connect the RMS millivoltmeter to "display output" pin 5 on the MA 2228/0.

14 - Adjust control R67 to obtain 0.7 V rms (2 V peak) on "display output" pin 5.

15 - Connect the RMS millivoltmeter to reproduce output (BNC connector).

16 - Inject a 1 V rms signal at 25 kHz (F. REF) on record input.

17 - Adjust F ref control R6 to obtain 1 V rms on reproduce output.

18 - Inject a 1 V rms signal at 150 kHz ($\frac{\text{F. MAX}}{2}$) on record input.

19 - Adjust $\frac{\text{F. MAX}}{2}$ control R13 to obtain 1 V rms on reproduce output.

20 - Inject a 1 V rms signal at 300 kHz (F. MAX) on record input.

21 - Adjust F. MAX control R8 to obtain 1 V rms on reproduce output.

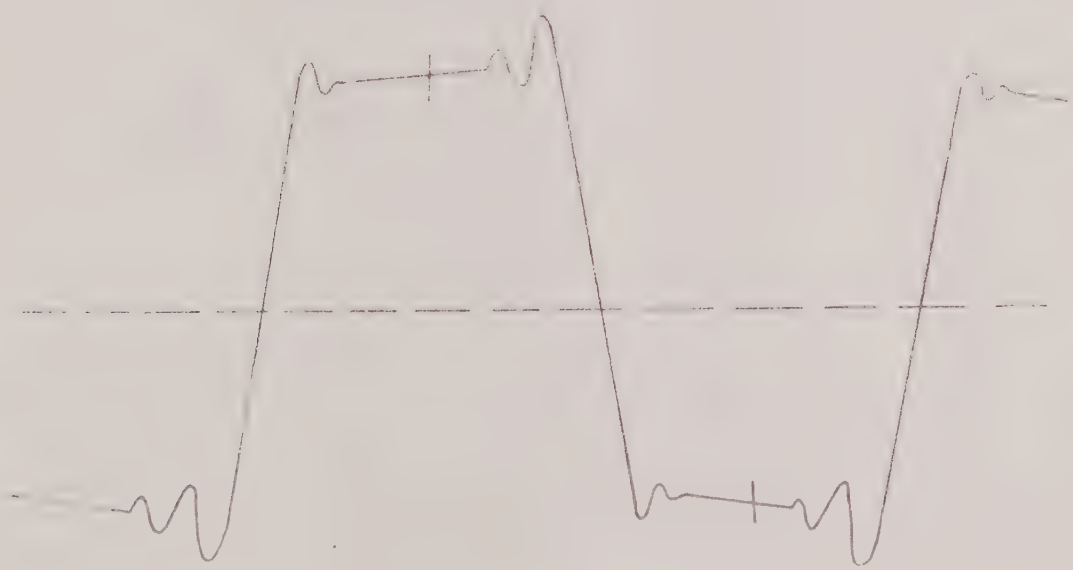
22 - Inject a 1 V rms sine wave signal at 75 kHz on record input (adjust third order harmonic level on control $\frac{\text{F. MAX}}{10}$), and set the frequency analyser at 100 %.

23 - Inject a 1 V rms sine wave signal at 25 kHz, adjust the frequency analyser, and finally adjust control R22 on the MA 2130/0 to obtain a distortion rate of 1 % on the analyser.

NOTE : This operation must be repeated several times.

24 - Inject a 3 V peak square wave signal at 15 kHz $\left(\frac{F.\ MAX}{20}\right)$ on record input (phase adjustment).

25 - Adjust PHASE control R14 to obtain a signal having the form shown below on reproduce output.



26 - Execute the following operations for the other tape speeds : 16 - 17 - 18 - 19 - 20 - 21 - 24 - 25 (see tables on following page).

27 - Return the recorder to its initial state.

Speed (cm/s)	F. REF. (kHz ± 10 %) Adjust on R6	F/2 (kHz) Adjust on R13	F MAX. (kHz) ± 3 dB Adjust on R8	F. MAX/20 (kHz) Adjust phase on R14
4.74	0.75	4.5	9	1
9.5	1.5	9	18	1
19	3	19	38	1.9
38	6	37	75	3.75
76	12.5	75	150	7.5
152	25	150	300	15
304	30	300	600	30

Speed (cm/s)	Bandwidth at ± 3 dB (kHz)	S/N ratio (dB)*
304	0.3 to 600	43
152	0.3 to 300	42
76	0.2 to 150	40
38	0.1 to 75	37
19	0.1 to 37.5	36
9.5	0.1 to 18	35
4.75	0.1 to 9	"(

* Measurement method as defined in IRIG document 118-73.

Nominal record current at all tape speeds, is that corresponding to a third order harmonic distortion level of 1 % (+ 10 %) of reference frequency at tape speed 152 cm/s (25 kHz), for an output level of 1 V rms on the terminals of a 600 Ω ± 10 % resistive load.

WBG2

Proceed as for WBG1 bandwidth adjustment, executing the following steps :

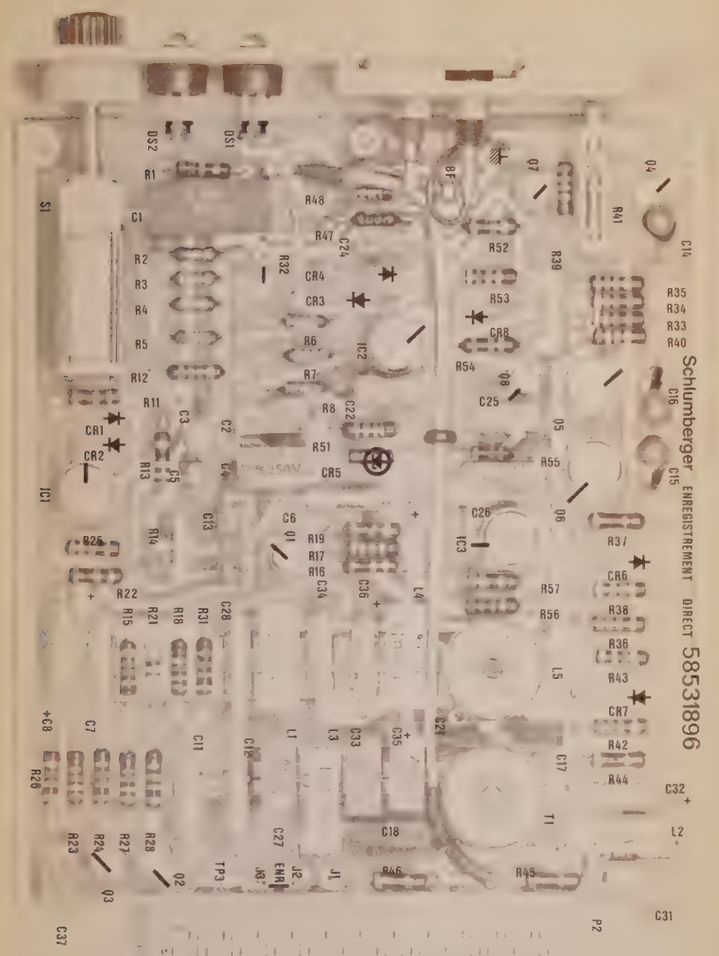
1 - 2 - 3
4 - Select standard and equalizers for WBG2.
5 - 6 - 7 - NOTE - 8 - 9 - 10 - NOTE
11 - Inject 1 V rms at 10 kHz.
12 - 13 - 14 - NOTES - 15
16 - Inject 1 V rms at 100 kHz.
17 - Inject 1 V rms at 100 kHz.
18 - Inject 1 V rms at 500 kHz
19 - Inject 1 V rms at 500 kHz
20 - Inject 1 V rms at 1 MHz.
21
22 - Inject 1 V rms at 300 kHz.
23 - Inject 1 V rms at 100 kHz and adjust on R21. - NOTE
24 - Inject 3 V peak at 50 kHz.
25 - 26 - 27

Speed (cm/s)	F. REF (kHz ± 10 %) Adjust on R6	F/2 (kHz) Adjust on R13	F. MAX (kHz) ± 3 dB Adjust on R8	F. MAX/20 (kHz) Adjust phase on R14
4.75	3.125	15	31	4
9.5	6.25	30	62	4
19	12.5	62	125	6.25
38	25	125	250	12.5
76	50	250	500	25
152	100	500	1000	50
304	200	1000	2000	100

Speed (cm/s)	Bandwidth at ± 3 dB **	S/N noise (dB)*
304	400 Hz to 2 MHz	26
152	400 Hz to 1 MHz	27
76	400 Hz to 500 kHz	27
38	400 Hz to 250 kHz	27
19	400 Hz to 125 kHz	26
9.5	400 Hz to 62 kHz	24
4.75	400 Hz to 31 kHz	23

* Nominal record current at all tape speeds is that corresponding to a third order harmonic distortion level of 1 %, at IRIG reference frequency for tape speed 152 cm/s (100 kHz), for an output level of 1 V rms on the terminals of a 50Ω ± 10 % resistive load.

**Normal tape run only.



Tensions alternatives en V et mV eff à 1000 Hz
AC Voltages in V and mV rms at 10000 Hz

Position 1V eff courant tête 1,8 mA
Entrée 1V eff
"1V rms" position *head current 1.8 mA rms*
"1V rms" input

entrée mesure *data input* P2 16 1V R1 220KΩ C 1µF R2 21KΩ R3 1,4KΩ R4 2,8KΩ R5 2,1KΩ R6 140Ω R7 280Ω R8 280Ω S1 0,1 0,5 1 5 10

C 2 10nF CR1 2_1N4448 CR2 R11 10KΩ IC1 µA709 R12 1,5KΩ C3 1000 pF C 5 56pF R 13 47Ω C4 10nF 100mV

LF gain adjust Réglage gainBF 22KΩ R14 C6 22µF R15 1,5KΩ R16 10KΩ R17 1,2KΩ R18 1,6KΩ R19 10KΩ Q1 2N2222 R21 75Ω

+12V -12V R32 150Ω

record +12V enregistrement R58 100Ω CR11 1N4448 P2 23 C38 22µF R27 1,6KΩ R28 430Ω Q2 2N2907 R31 430Ω C8 10µF C7 10µF R22 4,7KΩ R23 1,6KΩ R24 430Ω Q3 2N2222 R26 4,7KΩ C11 47µF C12 47µF C13 0,047µF R25 33KΩ R59 100Ω C39 22µF -12V enregistrement record

TP1 test ampli d'enregistrement *record amp test* 19

L5 84µH C21 120pF J2 J3 ENR RECORD P1 J1 P2 R46 10Ω C18 1200pF T1 C17 300pF R45 10Ω TP2

tête enre 30µH *record h*

TP3 test courant tête *head current test* soit 200mVeff *(200mV rms)*

+12V enregist. *record* L1 100µH 40mA C27 0,1µF C28 10µF

-12V enregist *record* L2 100µH 28mA C31 0,1µF C32 10µF

+12V L3 100µH 30mA C33 0,1µF C34 10µF

-12V L4 100µH 18mA C35 0,1µF C36 10µF C37 0,1µF

+12V enregistrement *record* R34 6,2KΩ R35 15KΩ C14 1nF Q4 2N2222 R33 6,2KΩ R41 1KΩ Réglage HF *HF adjust* R40 240Ω

R38 47KΩ CR6 1N4448 R37 10Ω R36 2,2KΩ C15 1nF Q5 2N2905 C16 1nF Q6 2N2219 R42 2,2KΩ R43 47KΩ CR7 1N4448 R44 10Ω

-12V enregistrement *record*

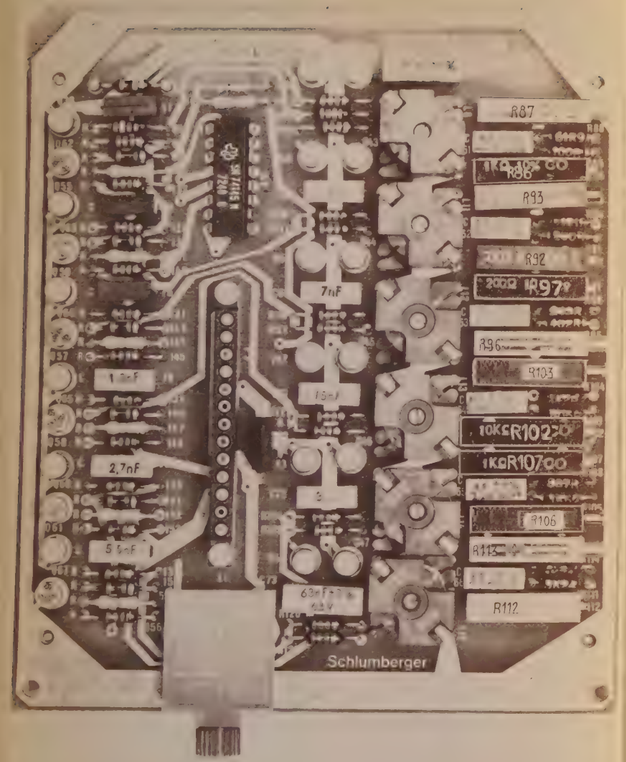
-12V R51 330Ω CR5 ZF 6 2

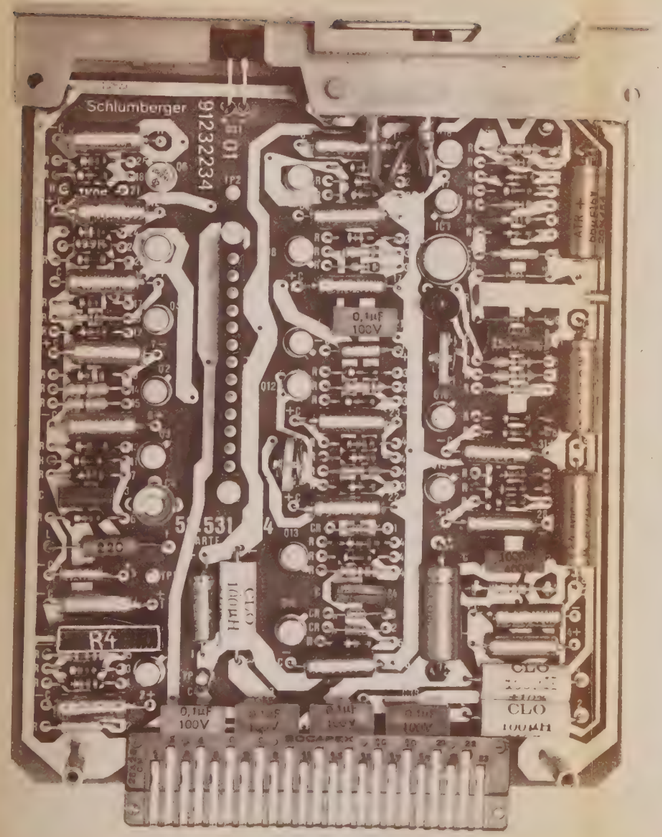
C22 10nF 100mV 2_1N4448 CR3 CR4 R47 158Ω IC2 uA710 R48 12,1KΩ C24 10nF

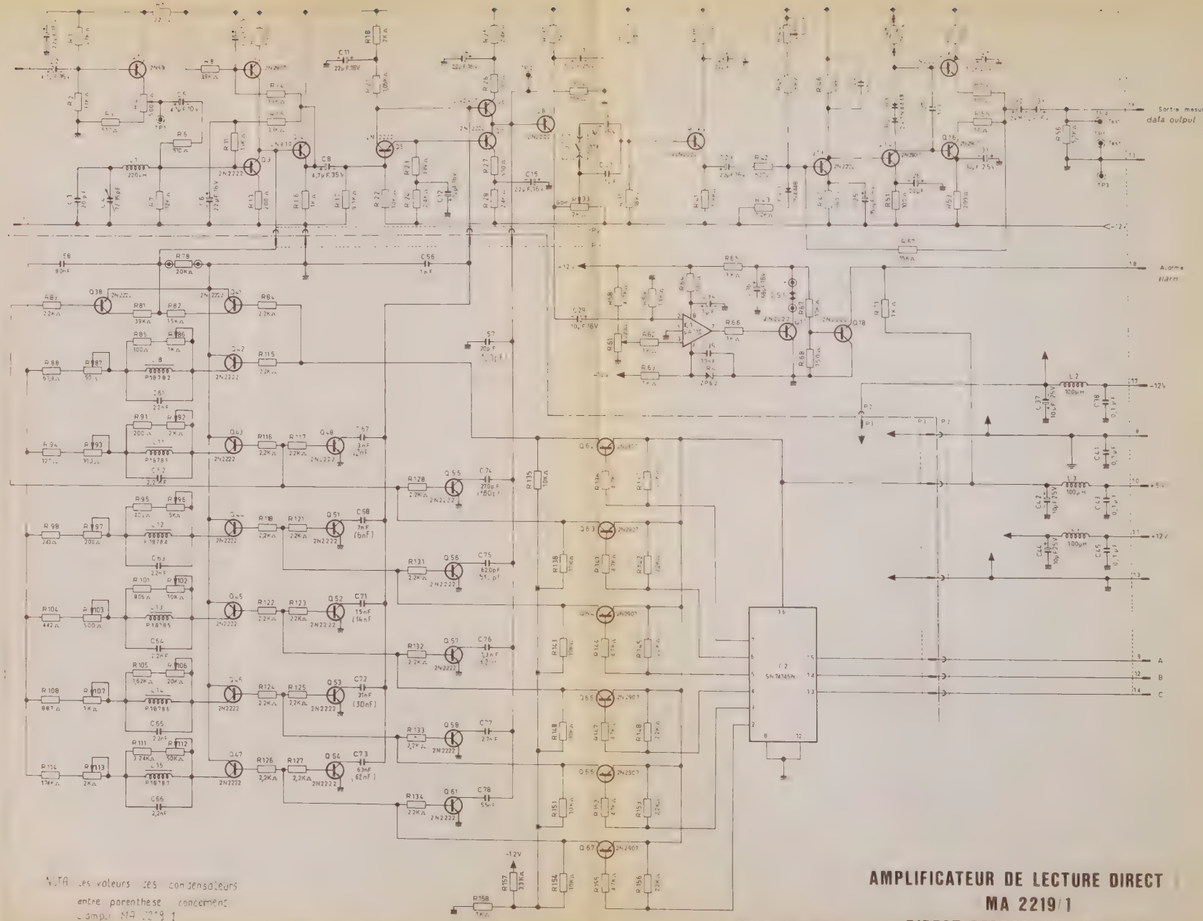
R5_1KΩ C7 2N2222 R53 620Ω SATUR. DS2 CR8 1N4448 R39 510Ω ALARM. DS1 Q8 2N2222 R54 1KΩ R55 1KΩ C25 10nF C26 10nF IC3 uA710 R56 12KΩ R57 51Ω +12V

Tensions alternatives HF en Vc.c. pour 20mA eff. dans la tête
HF AC voltages in Vpp, for 20mA rms head current

PI.7 - ENREGISTREMENT DIRECT MA 2114/0
MA 2114 DIRECT RECORD AMPLIFIER



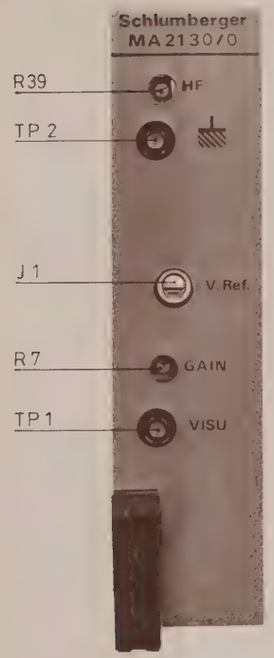



NOTA : les valeurs des condensateurs entre parenthèse concernent l'ampli MA 2219/1
Sortie mesure data output
Alarme alarm
-12V
+12V

AMPLIFICATEUR DE LECTURE DIRECT
MA 2219/1
DIRECT REPRODUCE AMPLIFIER

MT 5530 PI 9
MT 5528 PI 9

R 7 _ gain
R21 _ LBG 2 } réglage 1% H3
R22 _ B I
R39 _ réglage HF



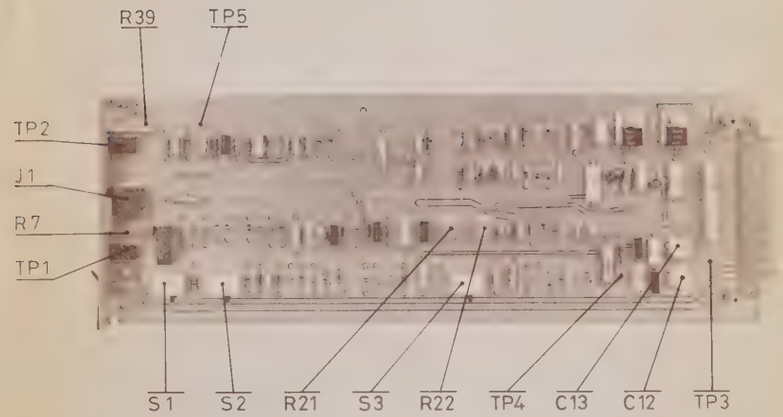
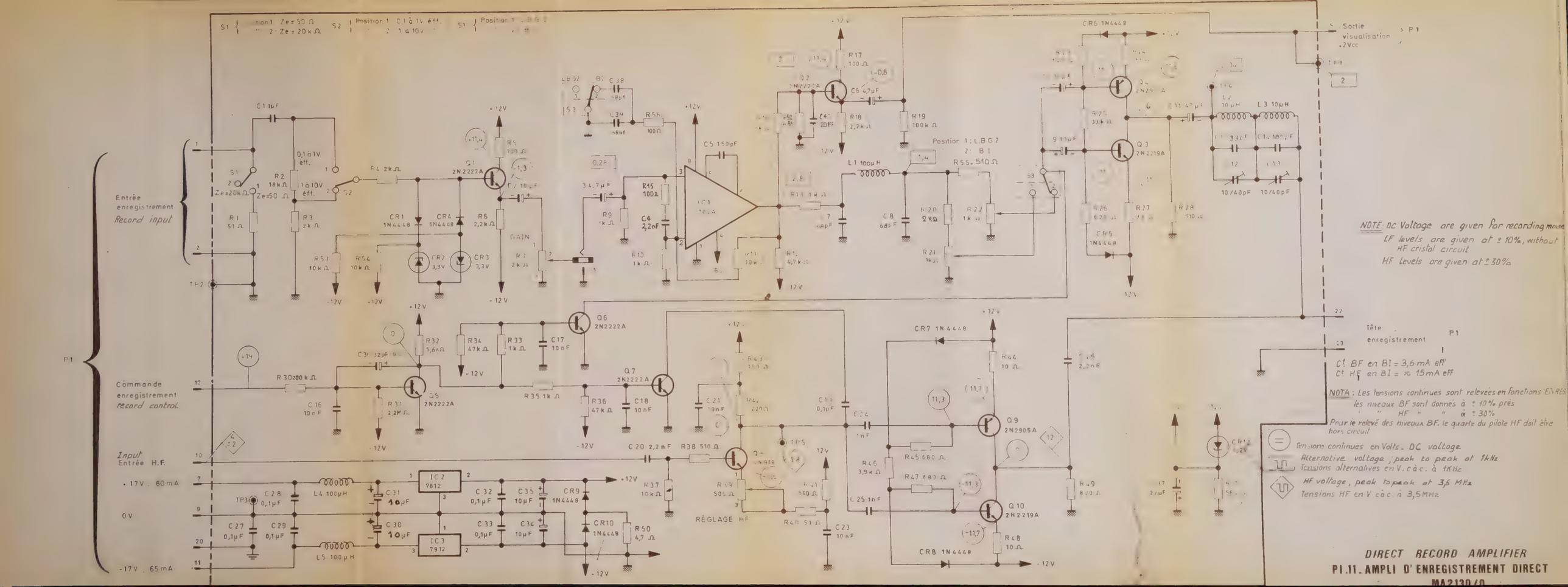


Fig 3.15


S1 1 : Ze = 50 Ω 2 : Ze = 20 kΩ
S2 Position 1 : 0,1 à 1V eff. 2 : 1 à 10V
S3 Position 1 : B G 2
Entrée enregistrement
Record input
Commande enregistrement
record control
Input
Entrée H.F.
+17 V . 60 mA
0 V
-17 V . 65 mA
P1
Sortie visualisation +2Vcc
Tête enregistrement
Ct BF en BI = 3,6 mA eff
Ct HF en BI = ≈ 15 mA eff
RÉGLAGE HF
Position 1 : L.B.G 2 : B I
GAIN
Tensions continues en Volts - DC voltage
Alternative voltage ; peak to peak at 1kHz
Tensions alternatives en V. c à c. à 1KHz
HF voltage, peak to peak at 3,5 MHz
Tensions HF en V c à c. à 3,5 MHz

NOTE : DC Voltage are given for recording mode
LF levels are given at ± 10%, without HF cristal circuit
HF Levels are given at ± 30%

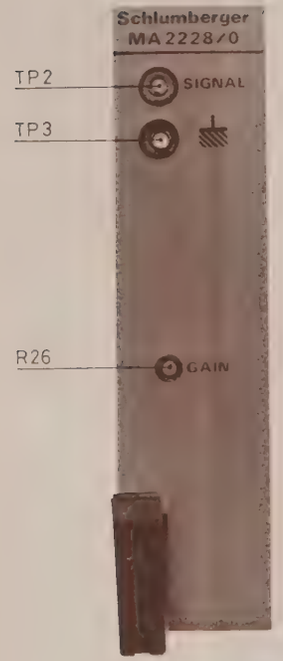
NOTA : Les tensions continues sont relevées en fonctions EN PF
les niveaux BF sont donnés à ± 10% près
" HF " " à ± 30%
Pour le relevé des niveaux BF. le quartz du pilote HF doit être hors circuit

DIRECT RECORD AMPLIFIER

P1.11. AMPLI D'ENREGISTREMENT DIRECT

MA2130/0

R26_ gain
R67_ niveau sortie visu
C4 _ 7 MHz
C5 _ 3,5 MHz } ajust. HF



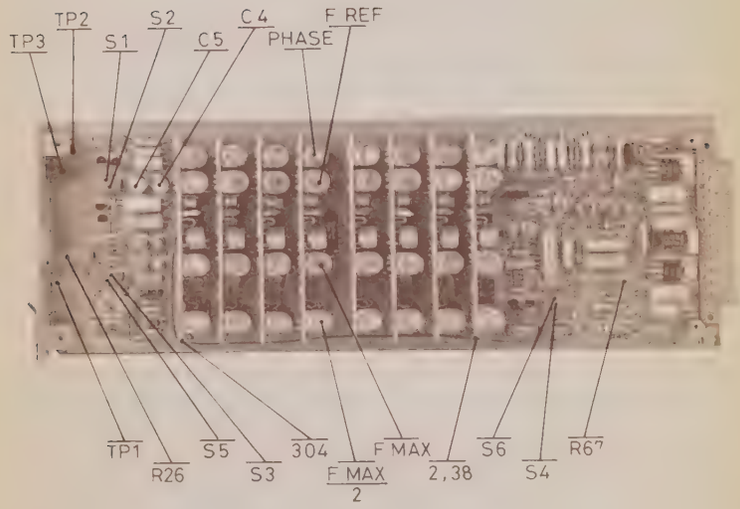
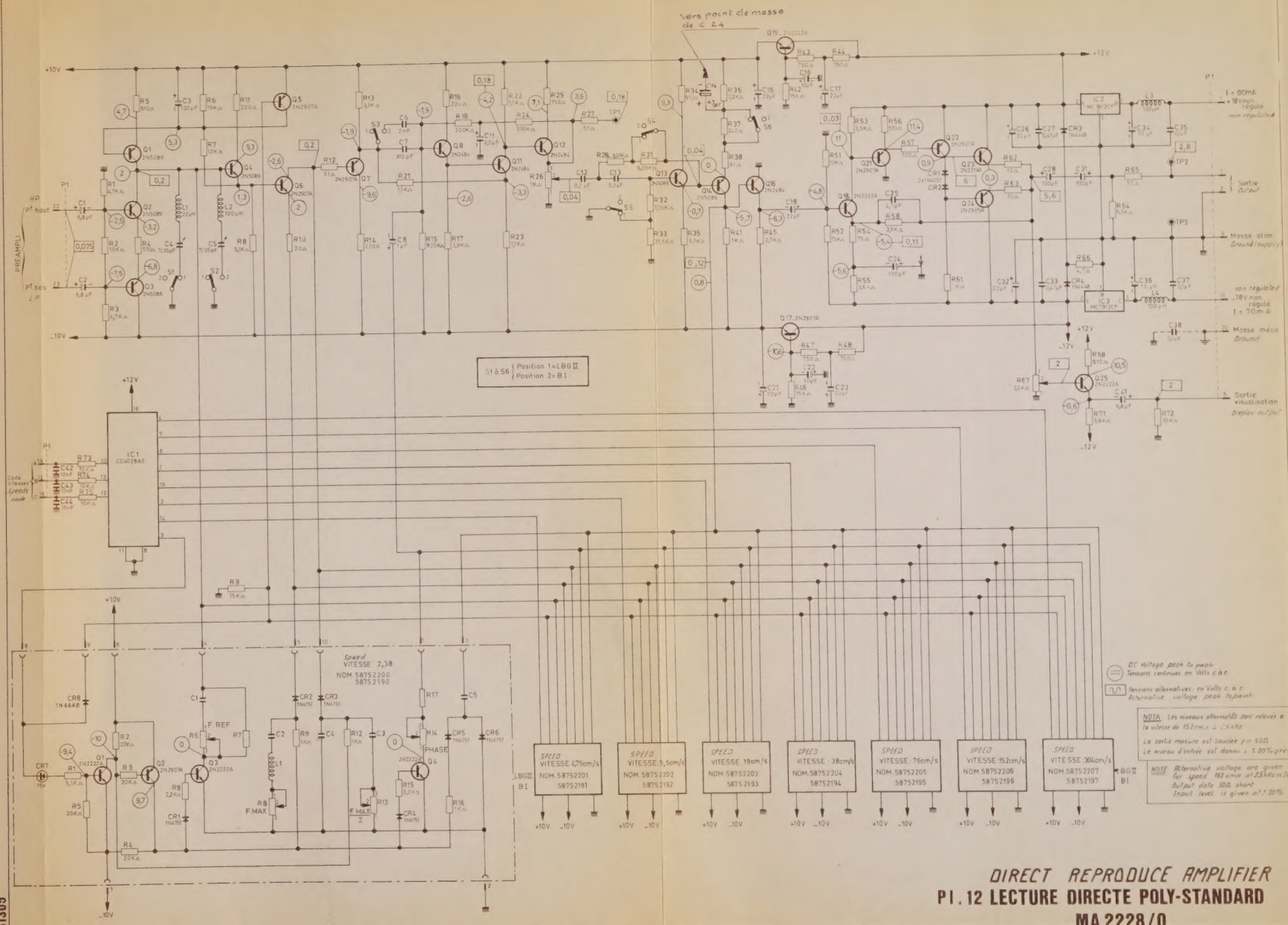


Fig 3.16


Vers point de masse de C 24
+10V
-10V
+12V
-12V
PREAMPLI
HP
pt haut
pt bas
LP
Position 1=LBG II
Position 2=B I
Code Vitesses Speeds code
Speed VITESSE 2,38 NOM. 58752200 58752190
F. REF
F. MAX
PHASE
SPEED VITESSE 475cm/s NOM. 58752201 58752191
SPEED VITESSE 9,5cm/s NOM. 58752202 58752192
SPEED VITESSE 19cm/s NOM. 58752203 58752193
SPEED VITESSE 38cm/s NOM. 58752204 58752194
SPEED VITESSE 76cm/s NOM. 58752205 58752195
SPEED VITESSE 152cm/s NOM. 58752206 58752196
SPEED VITESSE 304cm/s NOM. 58752207 58752197
LBG II
B I
Sortie Output
Masse alim. Ground supply
Masse méca Ground
Sortie visualisation Display output
DC Voltage peak to peak Tensions continues en Volts c à c
Tensions alternatives, en Volts c. à c. Alternative voltage peak to peak
NOTA Les niveaux alternatifs sont relevés à la vitesse de 152cm/s à 1,5kHz
La sortie mesure est soudée p.n. 520.
Le niveau d'entrée est donné à ± 20% près
NOTE Alternative voltage are given for speed 152 cm/s at 1,5kHz in the output data 580. short
Input level is given at ± 20%

DIRECT REPRODUCE AMPLIFIER

PI. 12 LECTURE DIRECTE POLY-STANDARD

MA 2228/0

11305

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1000426